Precision™ RTL Synthesis Release Notes

Software Release 2003a Update1

June 2003

End-User License Agreement
Trademark Information

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About These Release Notes

This manual contains release notes for the production release of Precision™ RTL Synthesis Release 2003a Update1. This manual also serves as a repository for Precision™ RTL Synthesis releases notes as they accrue over time.

From the time this document is published to the present, new information may have become available. Please refer to the following web-based documents for the most current information.
http://www.mentor.com/precision/download

Chapter 1
Introduction

Precision RTL Synthesis

Precision RTL Synthesis is a synthesis platform that maximizes the performance of both, existing programmable logic devices (CPLDs and FPGAs) and next-generation, multi-million gate field programmable system-on-chip (FPSoC) devices. Precision RTL Synthesis is a comprehensive tool suite, providing design capture in the form of VHDL and Verilog entry, advanced register-transfer-level logic synthesis, constraint-based optimization, state-of-the-art design analysis, schematic viewing and encapsulated place and route. Precision RTL Synthesis runs on Windows 98/NT/2000/XP; and UNIX Sun and HP platforms.

Note: For more information on the Precision RTL Synthesis standard features, options, and highlights refer to Chapter 1 in the Precision RTL Synthesis User's Manual.

System Installation

Refer to the Precision Synthesis Installation Guide for complete installation information.

Chapter 2
Release 2003a Update1

Customer-Reported Defects Fixed

In this update, the following customer-reported defects have been fixed:

Precision RTL Defects Fixed

dts0100122792 Precision removes black boxes

dts0100123267 Ungroup is causing Precision to not produce an EDIF

dts0100123246 Using (others=>'0') clause in component port mapping causes an error in compile

dts0100123278 Precision crashes during compile

Precision Physical Defects Fixed

dts0100121924 MGS_Design::get_tnm crashes when it finds an unconnected output pin

dts0100120798 crash in get_tnm -net

dts0100124830 Crash: Processing UCF File

dts0100121207 UCF2MGC:Error out when ucf instance contains char"-"

dts0100121111 Memory leak in report_timing

Chapter 3
Release 2003a

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Platform and FPGA Vendor Software Compatibility

This release is compatible with the following software and platform configurations:

- **Platforms:** PC NT/2000/XP; SUN Solaris 5.8; HP 11; Linux Redhat 7.3
- **Vendor Place and Route Software:** Xilinx ISE 5.2i SP1; ALTR Quartus II 2.2 sp1; LATTICE ispLever 3.0; ACTEL Designer R1-03

Release Highlights

Precision RTL 2003a enhancements include the following highlights. Further details are contained in these release notes.

Quality of Results and Controllability Improvements

- (All FPGA Vendors) Group/ungroup ASIC flow-style hierarchy control for incremental improvements in quality of results and ease of migrating designs from LeonardoSpectrum L3 flows to Precision flows
- (All FPGA vendors) Improved finite state machine control (FSM encoding algorithm manual override)
- (Altera and Xilinx users) Retiming optimization option that can improve design performance by up to 50%; Enhanced Register IO mapping
- (Xilinx users) Improved RAM inference

- (Altera) Enhanced Stratix device family support for MULT, MAC and RAM inferencing
- (Actel users) Radiation Hardened optimization support and updated timing models for improved timing correlation and accuracy

Expanded FPGA Vendor Device Support:

- (Lattice) Added ispMACH4000V family and updated device information for ispGDX2 devices
- (Xilinx) Virtex-II ProX, Spartan 3 device families; Added GT10 component support to Virtex-II Pro, added intelligent support for new differential signaling clock pads made available in ISE5.2i SP1. Continued to add most recent device family support
- (Altera) Enhanced Cyclone support to add EPIC4 devices; IO standard support for Stratix/GX, Cyclone, and APEX families

User Productivity Improvement

- (Xilinx users) New Xilinx UCF constraints flow for faster timing closure and improved timing correlation between synthesis and Xilinx Place and Route tools

Improvements for Military/ AeroSpace / High reliability applications:

- Support for Actel RADHard Optimization
- Ability to create “safe Finite State Machines”

Expanded Platform Support:

- Linux Redhat 7.3

  With this release Mentor Graphics provides production quality Linux support.

New Features

Mentor Graphics Licensing Upgrades to FLEXlm 8.2

The Mentor Graphics Licensing System has upgraded to Version 8.2 of FLEXlm. The supported licensing deamon is **mgcld**. You should update your license servers with this new deamon. The updated license server will continue to support all the older applications without any modification, however, an application using this updated version will not be able to acquire licenses from servers using older versions of FLEXlm. Additionally, new options have been added to the FLEXlm utility tools. For more information on the MGLS changes, refer to the document titled Release Notes for Licensing Mentor Graphics Software. For details on the 8.2 version of FLEXlm, refer to the FLEXlm End User Manual. These manuals can be accessed from the pulldown menu **Help > Open Manuals Bookcase**. For additional help, refer to the SupportNet knowledgeBase TechNote mg.51041.

Altera and Xilinx Quality of Results Improvement (Register Retiming)

Precision RTL Synthesis includes an option to invoke a powerful optimization algorithm called *register retiming* for improving performance in FPGA designs. Retiming allows the optimizer to move registers across combinatorial logic to improve circuit performance in situations where tight timing constraints exist. Improvements of up to 50% for Altera and Xilinx designs are not uncommon when using this algorithm.

Performing register retiming on a design will not change the functionality at the primary ports but may effect the observability of internal registers during post-synthesis simulation. For this reason, register retiming is an option that you can select to use prior to synthesizing your design. The option is not enabled by default; you must select **Retiming** through the **Tools Set Options… Optimization** dialog box. If observing internal registers during gate-level simulation is not an issue, you can feel comfortable enabling register retiming to solve timing issues. For more information on the retiming option, refer to the Precision RTL Synthesis Users Manual.

Altera Stratix Quality of Results

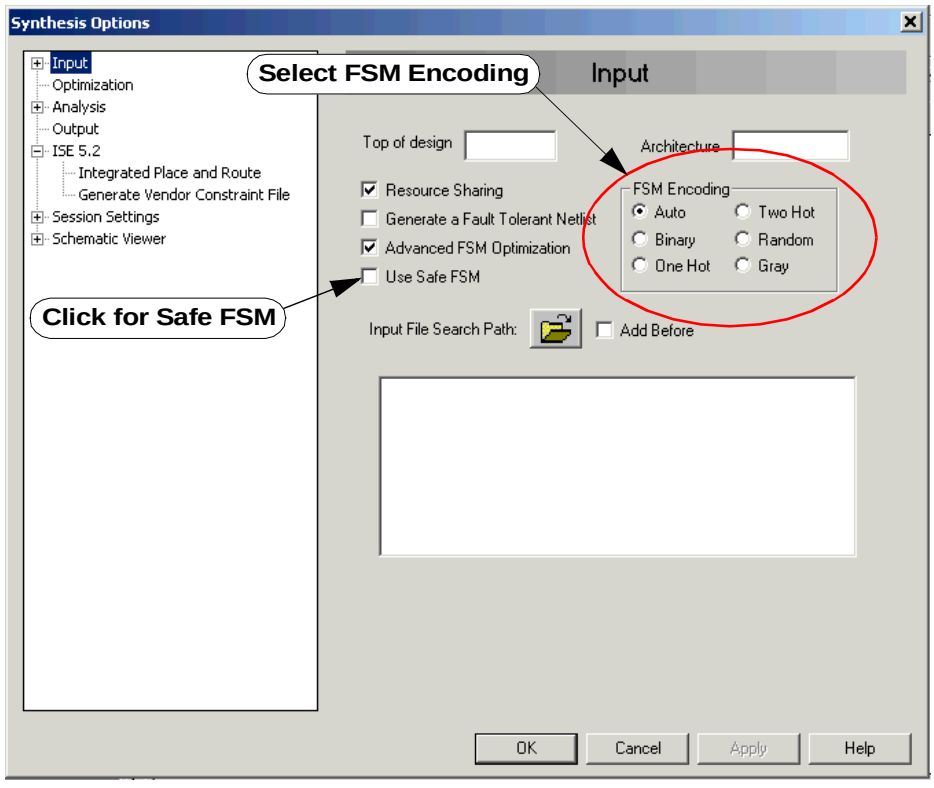
For Altera Stratix designs, Precision RTL now automatically chooses to use (infers) Multipliers, MACs and RAM memories when it deduces that these large FPGA elements are the best and most efficient way to implement your design. This can greatly improve the area and speed of your design.

State Machine Optimization Control (Safe State Machines, State encoding algorithm manual override)

Precision RTL now provides you with greater control over how state machines are implemented. This may be important to you if you are building high reliability designs. Precision RTL now provides you with the option to

- specify which state machine encoding algorithm you want the tool to use (for example “One Hot”)
- generate a “Safe” state machine. A safe state machine is a state machine in which a transition will always be to a valid state. Although state machine optimization will create a design which contains only valid transitions under normal circumstances, in safety critical situations where radiation could potentially change one of the bits, it is important to know that the state machine will recover at the next clock step into a valid state.

Safe FSM operation can be selected either from the GUI as shown below or by using attributes in your Verilog or VHDL source code. For more details on State Machine extraction and synthesis, refer to the Precision RTL Synthesis Style Guide.



Group and Ungroup Feature for Greater Controllability of Your Design Hierarchy and Improved Quality of Results

Precision RTL Synthesis now allows you to manipulate and control your design hierarchy using the group/ungroup commands. This feature allows you to dissolve hierarchy (merge more than one logical block into a single block) or create new hierarchy (split a logical block into more than one block). After doing so, you can re-optimize the new block or blocks created to improve results. In general, you will only need to use the group/ungroup features if your design is for some reason not meeting its performance or utilization objectives and you wish to manually control portions of the design that are to be incrementally improved. However, in the cases where you wish to group or ungroup hierarchy, you must follow these rules. To use this capability, do the following:

1. Invoke group/ungroup from the Precision command line interface or alternatively source group/ungroup commands from a script file (using the GUI “run script” command). There is no graphical user interface support for group/ungroup.

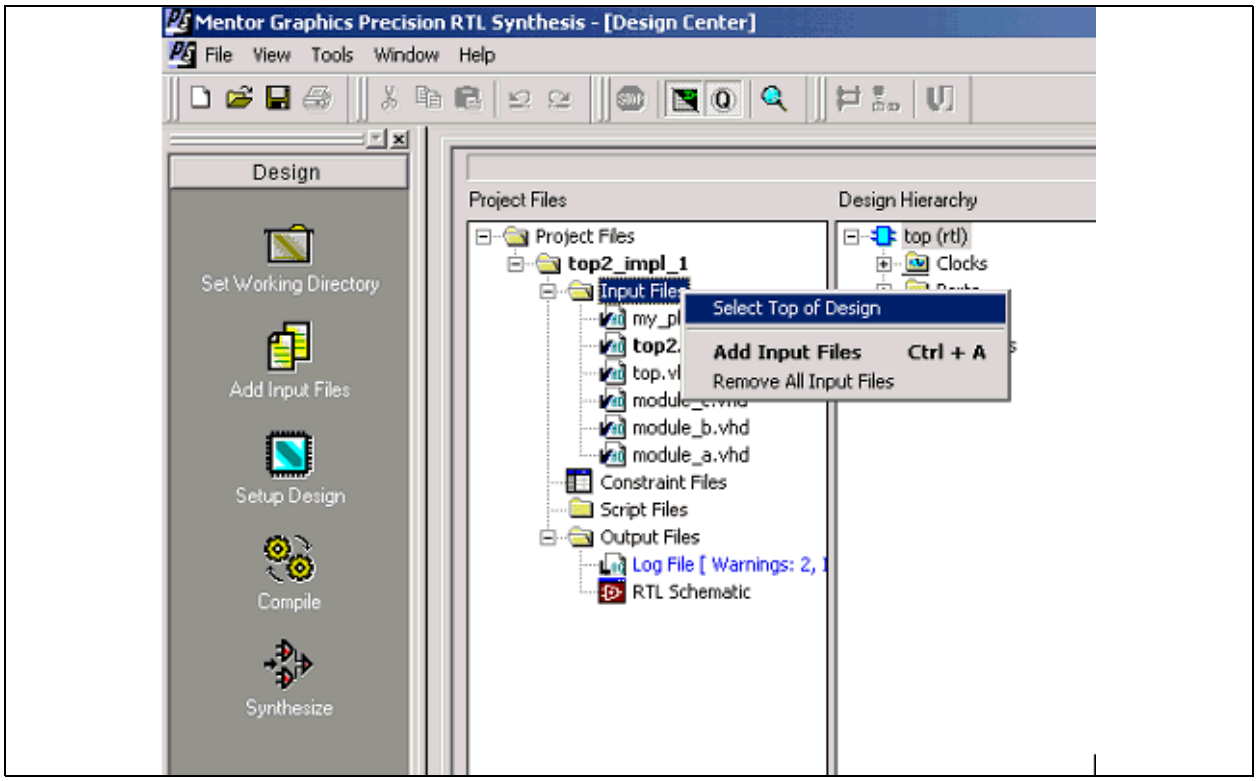
2. Grouping and ungrouping hierarchy should be performed after all design constraints have been applied and the design has been compiled. This will guarantee that the hierarchical references in the constraints remain valid when you recompile and incrementally synthesize the design.

3. Save your group/ungroup commands to a command file. Please note that these commands are not automatically saved into the project SDC file if you type them into the Precision RTL command line window. To save the group/ungroup operations performed, you must create a command file by selecting **File > Save Command File**. This file can then be edited to reuse the group/ungroup commands later, for example, as a script that is sourced using the **File > Run Script...** menu item.

For more detailed information of the use of the group/ungroup commands, refer to the Precision Synthesis Reference Manual.

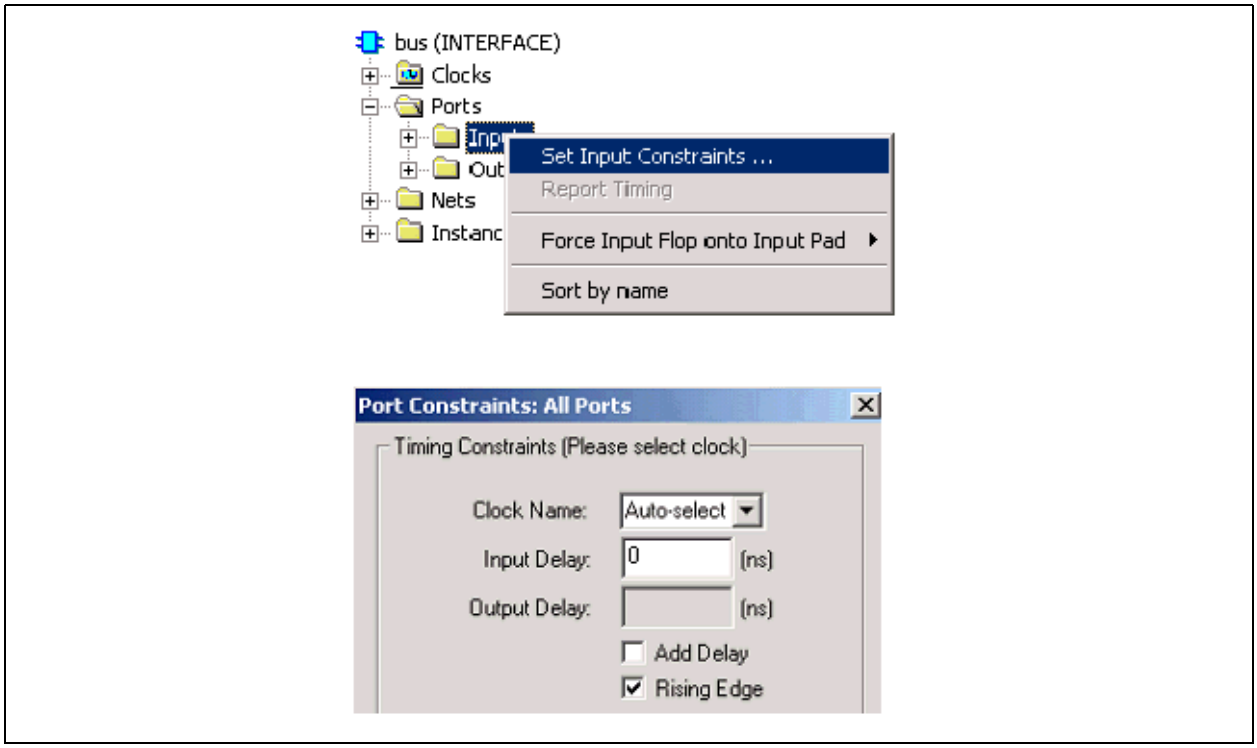
Automatic Detection of RTL “Top Level” Design File

Precision RTL Synthesis no longer requires that the top-level design file be placed at the end of your Input File List. After you have compiled the design, Precision will automatically detect the design top-level module file and create implementation folders and output files based on the top-level entity or module name. Precision will also allow design files to be arranged in the Input File List in any order, with the only exception being that VHDL packages must be placed before the files that reference them in the Input File List. If multiple design tops exist, Precision will select the last top read in the Input File List. After you compile the design, you can designate a top file in the GUI by right clicking on the Input Files folder, or individual input file, and then select the “Select Top of Design” menu option as shown in the picture below.



No Need to Specify Clock when Setting Input/Output Port Constraints on Buses

Precision Synthesis now allows you to set input/output port constraints on buses or ports folders without having to specify a clock. If the clock is not specified, the clock will default to “auto-select” and Precision will select the appropriate clock for generating the constraint. You need only to specify the input or output delay.



Actel Radiation-Hardened Implementation Support

Precision RTL has been enhanced to better support Actel RADHARD methodologies and implementations

Actel recommends and Precision RTL now fully implements three techniques for creating the logic of sequential elements in radiation-hardened FPGAs: Combinatorial-Combinatorial (C-C), Triple Mode Redundancy (TMR), and Triple Mode Redundant C-C (TMR_CC).

Combinatorial-Combinatorial (C-C)

The C-C technique provides a way to avoid using the radiation-soft S-module flip-flop by combining two combinatorial cells with feedback. For example, a DFP1 (comprised of two combinatorial modules) would be used in place of a DF1_CC macro.

Triple Mode Redundancy (TMR)

TMR is an acronym for triple-module-redundancy (or triple voting). It is a register implementation technique; each register is implemented by three flip-flops (or latches) that "vote" to determine the state of the register.

Triple Mode Redundant C-C (TMR_CC)

TMR_CC is also a triple-module-redundancy technique. Each voting register is composed of combinatorial cells with feedback (instead of flip-flop or latch primitives).

Steering Synthesis to use Radiation Hardened Implementations

To chose which method you want Precision RTL to use, set a "radhardmethod" attribute either on the reg/signal being driven by the flip-flop, the flip-flop instantiation itself, or on an entire module instantiation. Please see the TCL constraint example below.

A radiation-hardened implementation can also be set globally for the entire design by issuing the following command:

```
setup_design –radhardmethod=<one of “cc”, “tmr”, “tmr_cc”, or “none”>
```

The values that are valid for the radhardmethod attribute are identical to those recognized by the setup_design switch. Note that while attribute values are not case sensitive, setup_design switches are.

Example TCL constraint:

```
# Setting attribute on a flop in a TCL file refers to the flop itself
set_attribute -name radhardmethod -value tmr_cc -instance U1/reg_dataout

# Setting attribute on a module
set_attribute -name radhardmethod -value tmr -instance U2

# Setting rad hard method for the entire design
setup_design –radhardmethod=cc
```

Example Verilog Code:

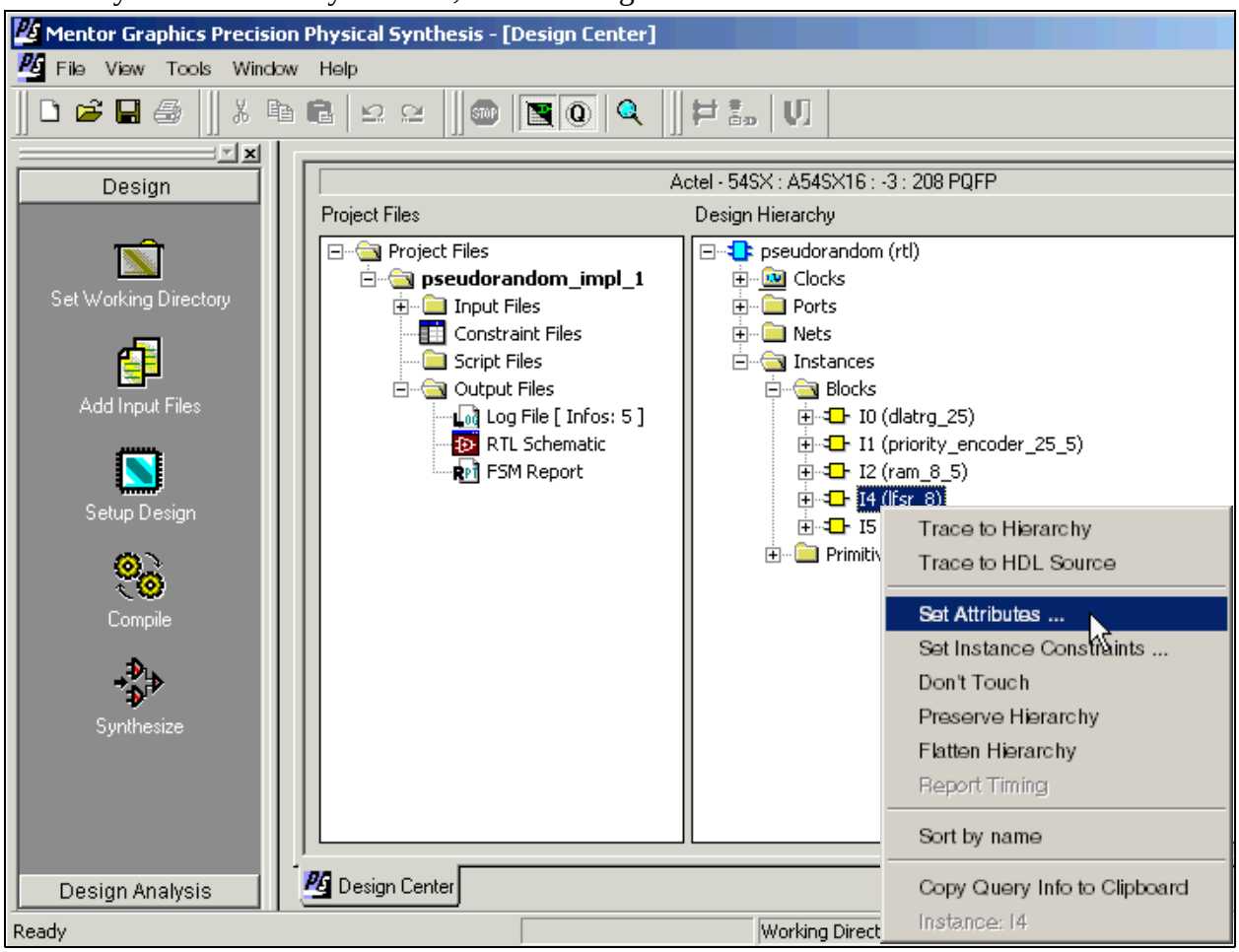
```
// Setting the attribute on a reg through a Verilog synthesis directive

reg [7:0] dataout;

// pragma attribute dataout radhardmethod tmr_cc;

// Setting the attribute on an instantiated module
// through a Verilog synthesis directive

// pragma attribute U2 radhardmethod tmr;
```

Example VHDL Code:

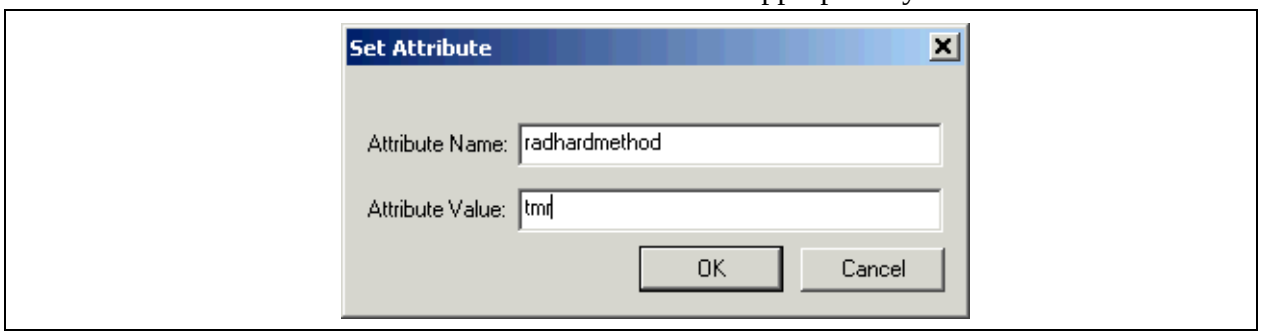
```
-- Setting the attribute on a registered signal through a VHDL attribute
--
attribute radhardmethod : string;
attribute radhardmethod of dataout: signal is “tmr_cc”;

signal dataout : std_logic_vector(7 downto 0);
--
-- Setting the attribute on an instantiated module
-- through a VHDL attribute
--
attribute radhardmethod : string;
attribute radhardmethod of U2: label is “tmr”;
```

Using the GUI to Set the RadHardMethod Attribute on an Object

You set the RadHardMethod Attribute by right-clicking on the design object in the Precision RTL Synthesis hierarchy browser, and selecting “Set Attributes…”



Under the User Attributes field, click on the New button and, as shown below, enter “radhardmethod” as the attribute name and set its value appropriately.



Altera Multicycle Path and False Path Constraint Support

Precision RTL Synthesis now supports multicycle path (MCP) attributes and false path attributes for Altera technologies, so that your timing reports reflect accurate timing results and identify true critical paths. The –from and –to MCP switches are also supported within these commands so that you can uniquely specify the exact false or multicycle path.

Precision allows you to specify multicycle or false paths between the following sets of objects:

- Port to instance
- Instance to port
- Instance to instance

Precision propagates these attributes by writing them in the Quartus-II Tcl file.

Since these attributes are applied on a point-to-point basis, they have to be set in the command line (after Compile).

```
set_multicycle_path “# cycles” –from “instance/port” –to “instance/port”
set false_path –from “instance/port” –to “instance/port”
```

Altera Timing Driven IOB Mapping

Precision now supports “Timing Driven IOB Mapping” for the Altera's Stratix and Cyclone family devices. By default, candidate registers are mapped into the IOE as long as they still satisfy the register to register timing. The advantage of doing the IOB mapping is to increase the availability of the device's internal registers (registers in the LEs) for other synchronous applications and also the reduced setup time and clock-to-out time. You can selectively unset the mapping by applying the `map_complex` attribute on individual ports or buses.

The following TCL command unsets the IOB mapping on a bus named accum_out

```
set_attribute -name map_complex -value false -port accum_out(*)
```

The "*" character is used as a wild card to represent the bus elements.

Change from Xilinx NCF File to Xilinx UCF File Constraints

Precision Synthesis now automatically generates a Xilinx UCF file after synthesis, rather than an NCF file. The reason is that NCF files can only constrain portions of the design that exist in your top-level EDIF file. Constraints for IP cores, or coregens, cannot therefore be specified adequately in NCF format. Constraints in the UCF file are applied after the entire design is input and linked. So the capabilities of the UCF file are a superset of those of the NCF file.

Using just UCF files in place of NCF also standardizes the passage of constraints from Precision and from other tools around a single format – UCF. This avoids confusion or conflicting constraints being passed to ISE place and route – In some situations UCF constraints not derived from Precision overrode the NCF constraints that Precision generated and the intent of these NCF constraints were therefore ignored by the ISE place and route tools, unbeknownst to the user.

Integrated IO Control for Altera and Xilinx

Precision Synthesis now allows you to set port attributes to control its IO properties - standard, slew rate and drive strength capabilities and pass this information on to the Place and Route tool. This feature is available for Xilinx and Altera technologies. Once set, Precision will propagate these attribute values to the respective place and route tools so that the correct IO information is used in place and route.

These attributes can be set both via the Precision GUI and also as attributes in the your HDL (Verilog or VHDL) code. For setting this attribute in the GUI mode, right click on the Ports folder and choose Set Input/Output Constraint. Assign the required IO standard, slew and drive by choosing from the pull-down menu.

Xilinx Differential Signaling Clock Buffer Support

Precision Synthesis supports new differential signaling clock buffers with differential outputs for advanced high-speed memory interfacing, including automatically adding the necessary global clock buffers such that the pad cell drives matched resources as recommended by Xilinx.

Xilinx Virtex-II Pro 3.3V LVCMOS IO Support

Precision Synthesis now supports use of the 3.3V LVCMOS IO standard recently added to the Virtex-II Pro product offering through the use of SelectIO attributes. The user selects these IOs using the IO_STANDARD attribute.

Xilinx Asynchronous Register Support

Precision Synthesis supports passing the `async_reg` attribute either from the VHDL source code, or applied as an attribute on registers through a constraint file or script. A register tagged with this attribute will be modeled such that if a timing violation occurs during post-layout simulation, it retains its previous value instead of propagating an 'X'. This attribute is passed to Xilinx so that X propagation is disabled for asynchronous registers to prevent simulation failures.

New Xilinx Flip Flop Mapping Algorithm for IO Registers

This capability allows you to selectively trade off product performance on and off chip. By default, Precision RTL Synthesis creates a design by implementing boundary flop flops as part of the chip IO Blocks where ever possible, regardless of the design's desired clock frequency. This includes transforming inverted inputs and outputs to normal flip flops with inverted reset states. New attributes have been added to allow you to disable this mapping on a flop-by-flop and IOB-by-IOB basis. This functionality is available for the following Xilinx device families: Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Spartan-II, Spartan-IIE, and Spartan-III devices.

To use, set one of the following three new Precision Synthesis attributes to false:

Inff (FOR INPUT PORTS)
Outff (FOR OUTPUT PORTS)
Triff (FOR TRISTATE PORTS)

It is only necessary to set these attribute values on those flip flops that you do not want mapped into the IOB (by setting the appropriate inff, outffF, or triff attribute to false).

You can set these attributes as part of a script by using commands of the following format in your SDC constraints file:

```
set_attribute -name inff -value false -port <port_name>

set_attribute -name outff -value false -port <port_name>

set_attribute -name triff -value false -port <port_name>
```

Customer-Reported DRs Fixed

DR329428 Precision Synthesis unable to properly link EDIF input files.

DR331589 Customer design causes Precision to generate an out of memory error.

DR333540 Precision Synthesis fails to generate correct VHDL output for simulation of customer design.

DR329428 Precision Synthesis unable to properly link EDIF input files.

DR331589 Customer design causes Precision to generate an out of memory error.

DR333540 Precision Synthesis fails to generate correct VHDL output for simulation of customer design.

DR333996 Precision Synthesis abnormally terminates on customer design.

DR334165 Precision Synthesis claims to run out of room in a targeted Virtex-II device before it actually does.

DR334345 Precision Synthesis results don’t match customer’s expectations after Quartus II P&R.

DR334538 Precision Synthesis improperly mapping to I/O flip flops in Stratix device.

DR334826 Using an improper coding style for RAM inferencing causes Precision Synthesis to crash. Precision should issue a warning message instead.

DR334926 Precision Synthesis fails to write a blackbox netlist because the design contains no gates.

DR335366 Precision Synthesis autowrite not working properly on customer design.

DR335895 Precision Synthesis unable to read netlist that was written by the Precision netlist writer.

DR336322 Precision Synthesis fails to implement TMR on some flip flop when targeting Actel ACT2RT device.

DR337164 Precision Synthesis creates incorrect FSM logic for customer design.

DR338594 Precision Synthesis abnormally terminates on customer design while exercising the retiming algorithm.

DR338614 Precision Synthesis incorrectly infers a selcounter for a customer design.

DR338688 Precision Synthesis abnormally terminates when customer's Stratix design is synthesized without IO pads.

DR338913 Precision Synthesis abnormally terminates on customer design during the compile phase.

DR338934 Precision Synthesis generates a design that is way larger than expected.

DR339076 Precision Synthesis generates an unrecognizable value for the Xilinx `FACTORY_JF` attribute.

DR339080 Customer unable to complete place and route with LogicLock flow.

DR339258 Precision Synthesis abnormally terminates on customer design after a large number of pin constrains are entered via the GUI.

DR339615 Precision Synthesis abnormally terminates on customer design during Advanced FSM optimization.

Chapter 4
Release 2002d update1

Customer-Reported Defects Fixed

In this update, the following customer-reported defects have been fixed:

DR336322 The Precision Synthesis ACT2RT library fails to implement TMR on some flip-flops.

DR336651 Unsupported Verilog 2001 functions $signed() and $unsigned() generate an unclear error message which could cause the user to overlook a possible bad logic issue.

DR337010 Precision RTL Synthesis produces incorrect results for a customer design.

DR337164 Precision RTL Synthesis produces incorrect results for a customer design.

Chapter 5
Release 2002d

From the time this document is published to the present, new information may have become available. Please refer to the following web-based release notes for the most current information. http://www.mentor.com/precision/download

New Features

Precision RTL Synthesis is focused on delivering 1) An Intuitive User Interface, 2) Excellent Quality of Results, and 3) Advanced Design Analysis capability. The new features of this released are highlighted under these three categories.

Intuitive User Interface

Project Management

A new Project Management system has been added that facilitates multiple implementations of a design. This new capability enables you to save “snapshot” versions of your design for possible restoration later and perform easy "what if?" analysis with various versions of your design.

Extended Help from the Transcript Window

The online help system has been extended to provide quick access to command reference information from the Transcript window. You can now “double click” on a transcripted command to bring up the command reference page on that command.

Verilog 2001

For the third release in a row, Verilog 2001 constructs have been extended. Support for the signed shift operator and named parameters has been added.

Actel and Lattice Integration

You can now review the results of running Actel and Lattice Place and Route tools directly from the Precision user interface. This allows you to run a completely integrated synthesis flow through the place and route from within the Precision environment.

Excellent Results

Tighter correlation to Place and Route

The accuracy of pre place and route timing estimates has been greatly improved, providing much closer correlation between Precision's PreciseTime Analysis features and post place and route reports, saving lengthy design iterations. Note, however, that your pre place and route reports may indicate that your design has apparently degraded in performance, compared with earlier Precision RTL release timing reports. In benchmarking situations, it is always recommended that you judge quality of results from post place and route timing data.

Altera Stratix Retiming

Altera Stratix support has been enhanced by adding a new Retiming feature. This can increase performance by up to 15% on designs that benefit from this functionality.

Xilinx RAM Inference

For the third release in a row, Precision's automatic RAM inferencing has been extended, which helps to eliminate the time consuming need to manually instantiate memories.

Advanced Design Analysis

Extended SDC Support

This release extends the support of Synopsys Design Constraints to help focus optimization on true critical paths for better quality of results. With this release, Precision now supports the set_max_delay and set_min_delay exception constraints.

Precision Physical Synthesis 2002d Highlights

The 2002d release is the second release of Precision Physical Synthesis. This release focuses on further improving the performance of Xilinx Virtex-II and Virtex-E designs that may have been constrained outside of the Precision RTL synthesis environments and designs that may have been started from within an alternative synthesis tool.

Xilinx UCF file Constraint Translator

A new UCF to SDC constraint translator has been added that helps convert user design constraints added during place and route, to design constraints readable by Precision Physical Synthesis. This new feature facilitates better timing correlation between synthesis and place and route for faster timing closure.

Customer-Reported DRs Fixed

DR330543 Precision RTL Synthesis does not map memory to ESBs.

DR330733 Precision RTL Synthesis abnormally terminates on a customer design without a transcript explanation.

DR330810 Customer design with 3-D arrays on ports causing Precision RTL Synthesis to produce an incorrect EDIF netlist for Xilinx.

DR331781 Precision RTL Synthesis stalls on customer design.

DR331921 Virtex-II design fails in synthesize in Precision RTL due to untranslatable nets.

DR332338 Precision RTL Synthesis connecting the wrong bits of a multiplier to the outputs of a Virtex-II design

DR332767 Precision RTL Synthesis abnormally terminates while compiling a customer design

DR332832 Precision RTL Synthesis is incorrectly compiling input files located in different source directories.

DR333044 Precision RTL Synthesis abnormally terminates on a customer design during FSM extraction.

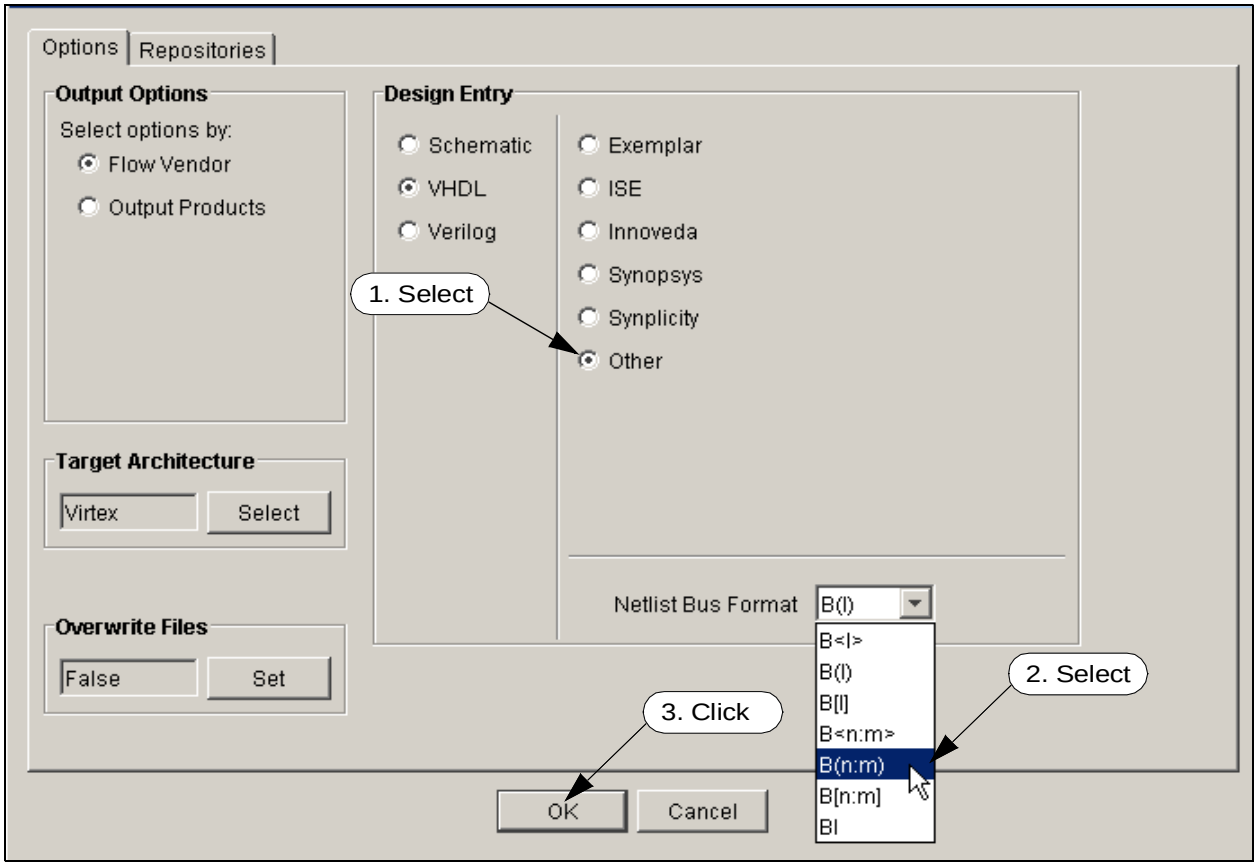
Known Issues

EDIF Netlist Issues

Specifying the Correct Bus Format in Xilinx CORE Generator

If you are using the Xilinx CORE Generator to generate a module, make sure that you specify the **B(m:n)** bus format which is compatible with Precision. The Figure below illustrates how to set the bus format with the CORE Generator **Project > Project Options** dialog box.

Figure 5-1. Xilinx CORE Generator Project Options Dialog Box



If **Exemplar** is selected, the format will be wrong for Precision because it will be a bit-based format.

Reference to “Work” Library in EDF File Not Treated Correctly

The current Precision EDIF netlist parser treats a **libraryRef** of ‘work’ incorrectly. If the libraryRef property is set to 'work' then the last EDF file containing the library will always completely replace a previous occurrence of the 'work' library. This is not a problem when the

libraryRef property is set to another name. For example, if you are reading multiple EDF files with the same libraryRef “work” and the first EDF file contains the module definition called “compare” and the second EDF file also has a “compare” but this is a black box definition, then “compare” is not properly expanded and remains a black box. An indication of the issue is when a large number of instances are not found when reading the XDL file. The work around is to change and duplicate libraryRef properties to new names.

LUT Instance as Part of a Black Box Not Treated Correctly

If a LUT instance is part of the black box or a module with a `dont_touch` attribute, the EDIF writer writes out the following: (property EQN (string "()"))". This causes the EDIF reader to stop with an Error “invalid LUT equations”. The way to correct this is to edit the EDIF netlist and put the following into the equation. (property EQN (string "(IO * !IO)"))". This will be corrected in a future release.

Chapter 6
Release 2002c

From the time this document is published to the present, new information may have become available. Please refer to the following web-based release notes for the most current information. http://www.mentor.com/precision/download

New Features

Improved Quality of Results

This release of Precision RTL Synthesis includes eleven significant QoR enhancements. Areas of improvement include improved RTL and RAM Inferencing, IO driver sizing, IOB mapping and Virtex and Stratix synthesis. During testing, 30% of the Xilinx designs showed quality improvements and 55% of the Altera designs showed quality improvements.

Improved Run Times

Run times for this release show an average 40% improvement. Large hierarchical designs show the greatest run time improvement.

Enhanced Verilog 2001 Support

Verilog 2001 support has been enhanced to include the following addition constructs:

- Power (Exponential) Operator
- Automatic Width Extension Past 32 Bits
- Reg Declaration with Initialization
- Signed/Unsigned Parameters

Support for Altera PLL Clock Propagation

Clocks now propagate through Altera PLL cells, including the clock multiplication and division outputs.

Improved Timing Correlation to P&R

As shown below, Precision timing analysis now takes into account the effects of clock skew. This improves the correlation to the place and route timing reports.

```
Critical path #1, (path slack = 2.45):

SOURCE CLOCK: name: clk period: 10.000000
     Times are relative to the 1st rising edge
DEST CLOCK: name: clk period: 10.000000
     Times are relative to the 2nd rising edge

NAME                          GATE                  DELAY    ARRIVAL DIR
I4_I1_reg_done_rcving_reg/C FDCE                              0.00   up
I4_I1_reg_done_rcving_reg/Q FDCE                    0.71      0.71   up
ix297/I0                    LUT2                              0.71   up
ix297/O                     LUT2                    0.47      1.18   up
int_obuf/I                  OBUF(LVTTL,SLOW,12)               1.18   up
int_obuf/O                  OBUF(LVTTL,SLOW,12)     5.16      6.34   up
in (port)                                                     6.34   up

                            Initial edge separation:      10.00
                            Source clock delay:       -     1.20
                                                      ---------
                            Edge separation:              8.80
                            Setup constraint:         -     0.00
                                                      ---------
                            Data required time:           8.80
                            Data arrival time:        -     6.34
                                                      ---------
                            Slack:                        2.46
```

New Technologies Supported

Actel Technologies

All Actel technologies including the new “Axcelerator” family of devices are supported.

Lattice Technologies

All Lattice technologies including the new ORCA 4 and ixpXPGA devices are supported.

Altera Cyclone

The following Altera Cyclone devices are supported.

Altera Cyclone Devices	
EP1C3	T100C, T144C
EP1C6	T144C, Q240C
EP1C12	Q240C, F324C
EP1C20	F324C, F400C
Speed Grades supported: 6, 7, 8	

Customer-Reported DRs Fixed

DR323866 Precision RTL Synthesis abnormally terminates on customer design.

DR324224 Need to add messages telling why a dialog entry box is greyed-out.

DR328119 Need to connect unused LCELL inputs to a default value.

DR328463 Can’t read EDIF netlist written with Synplicity EDIF writer.

DR328775 Precision “Save > Project” dialog box should provide a default project name.

DR330009 Precision RTL Synthesis abnormally terminates on customer design.

DR330259 Precision inferring wrong reset type in pipelined multiplier.

DR330581 In Precision, Synplify attribute “syn_noclockbuf” turns buffering on instead of off.

DR330585 The colored Info/Warning/Error dots in the Code Browser disappear on recompile.

DR330614 Need a folder under instances in the Design Browser that contains all black boxes.

DR330733 Precision RTL Synthesis abnormally terminates on customer design.

DR330790 Precision RTL Synthesis abnormally terminates on customer design.

Known Issues

Invalid Input Buffer Choices for Virtex-II/Virtex-II Pro

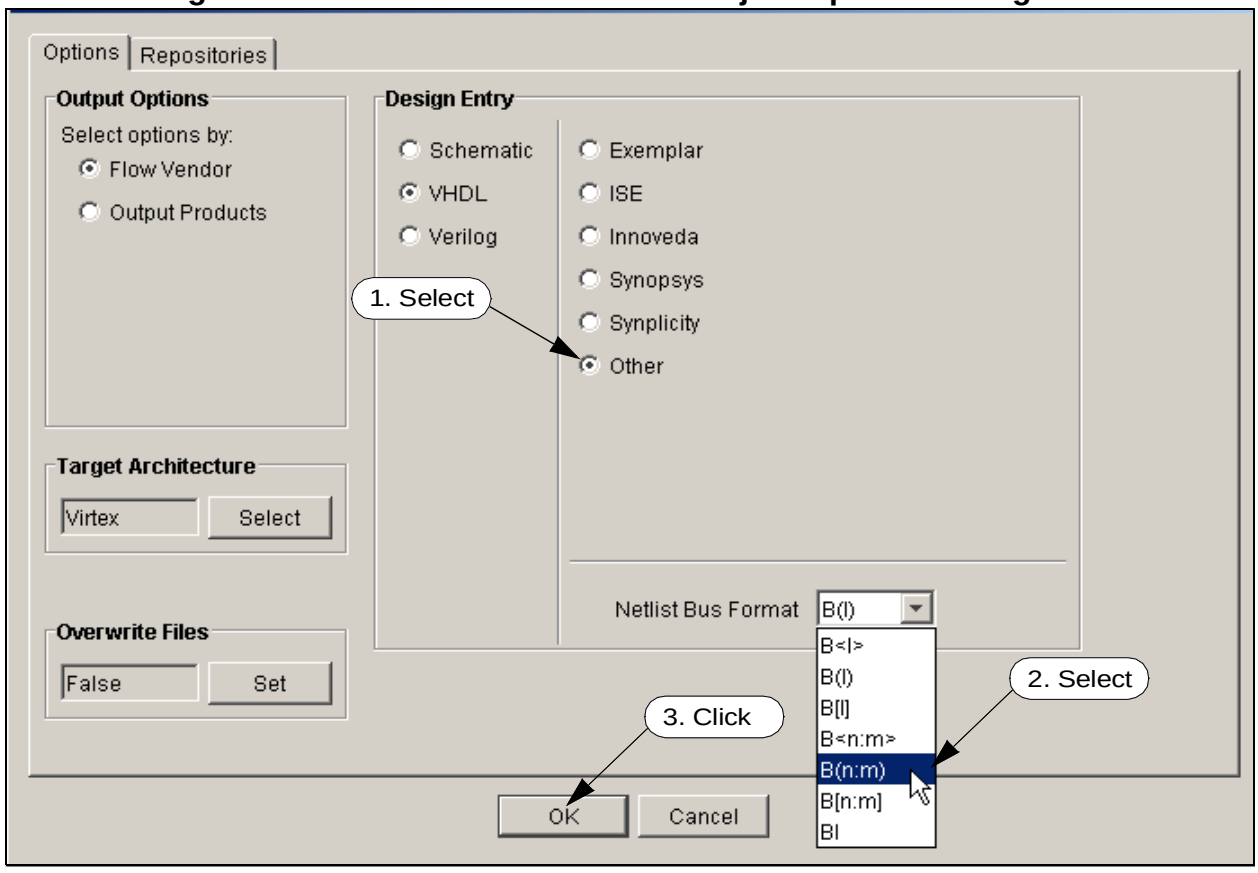
The Precision GUI currently presents a few invalid input buffer choices for Virtex-II and Virtex-II Pro technologies. If you assign one of these invalid buffers to an Input Port, Xilinx ISE will report an error in Ngdbuild. The input buffers with a drive and slew attribute appended to the name are invalid. For example, the buffer IBUF_LVCMOS_25 is valid, however the buffer IBUF_LVCMOS_25_F_12 is invalid and the buffer IBUF_LVCMOS_25_S_12 is invalid.

EDIF Netlist Issues

Specifying the Correct Bus Format in Xilinx CORE Generator

If you are using the Xilinx CORE Generator to generate a module, make sure that you specify the **B(m:n)** bus format which is compatible with Precision. The Figure below illustrates how to set the bus format with the CORE Generator **Project > Project Options** dialog box.

Figure 6-1. Xilinx CORE Generator Project Options Dialog Box



If **Exemplar** is selected, the format will be wrong for Precision because it will be a bit-based format.

Reference to “Work” Library in EDF File Not Treated Correctly

The current Precision EDIF netlist parser treats a **libraryRef** of ‘work’ incorrectly. If the libraryRef property is set to 'work' then the last EDF file containing the library will always completely replace a previous occurrence of the 'work' library. This is not a problem when the libraryRef property is set to another name. For example, if you are reading multiple EDF files with the same libraryRef “work” and the first EDF file contains the module definition called “compare” and the second EDF file also has a “compare” but this is a black box definition, then “compare” is not properly expanded and remains a black box. An indication of the issue is when a large number of instances are not found when reading the XDL file. The work around is to change and duplicate libraryRef properties to new names.

LUT Instance as Part of a Black Box Not Treated Correctly

If a LUT instance is part of the black box or a module with a `dont_touch` attribute, the EDIF writer writes out the following: (property EQN (string "()"))". This causes the EDIF reader to stop with an Error “invalid LUT equations”. The way to correct this is to edit the EDIF netlist and put the following into the equation. (property EQN (string "(IO * !IO)"))". This will be corrected in a future release.

Invoking Quartus II Multiple Times

Invoking multiple Quartus II 2.1 SP1 sessions at the same time may cause one or more of the sessions to hang. Mentor Graphics is working with Altera to identify the source of the problem.

Un-used Ports on Sub-Modules in a Block-Based Synthesis Flow will Cause P&R to Fail

If you are using a block-based (bottom-up) synthesis flow and there is an un-used port on one or more pre-synthesized blocks, the design will fail in Place and Route. Contact Mentor Graphics Customer Support for possible workarounds.

Chapter 7
Release 2002b

New Features

Precision Moves to MainWin 4.02

MainWin is the software package that provides a Windows platform on the Unix operating system. With this release, Precision RTL Synthesis has moved to MainWin 4.02.

Sun Solaris 7 No Longer Supported

With the move to MainWin 4.02, the Sun Solaris 7 Operating System is no longer supported. Precision RTL Synthesis will, however, continue to support Solaris 8, HP-UX 11.00 and Windows 98/NT/2000/XP.

Initial Support for Verilog 2001

This release of Precision RTL Synthesis provides initial support of Verilog 2001. The features supported are as follows:

- Signed/unsigned
- Comma separated sensitivity list
- Combinational sensitivity list
- Combined port/data type
- ANSI-style port lists

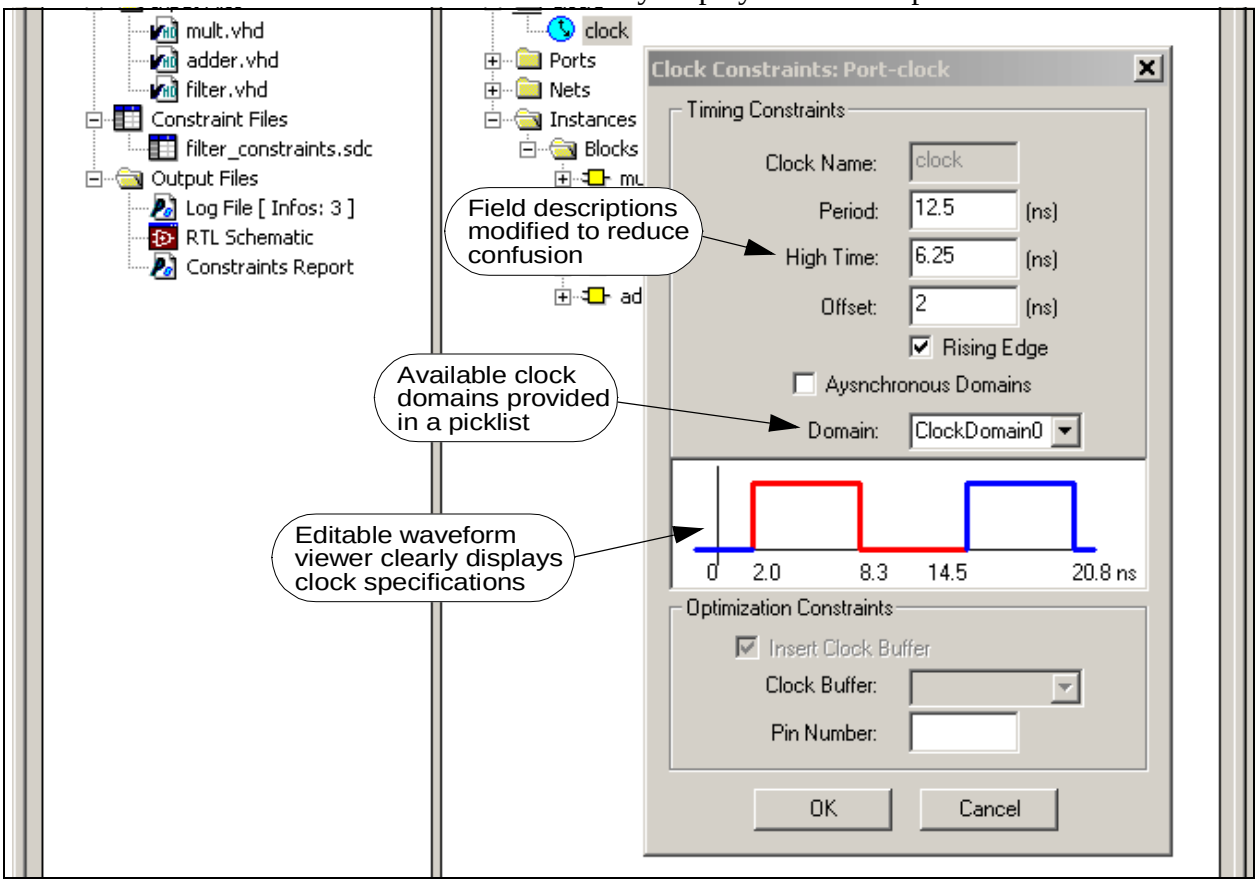
New Toolbar STOP Button

A new STOP button has been added to the Toolbar that allows you to halt the execution of the Compile and Synthesize commands.

Improved Clock Constraint Dialog Box

A new Clock Constraints dialog box as been added with the following enhancements:

- Modified field descriptions to reduce confusion
- A new Domain picklist for specifying an available clock domain
- an Editable waveform viewer that clearly displays the clock specification.



Xilinx RAM Inferrencing Enhancements

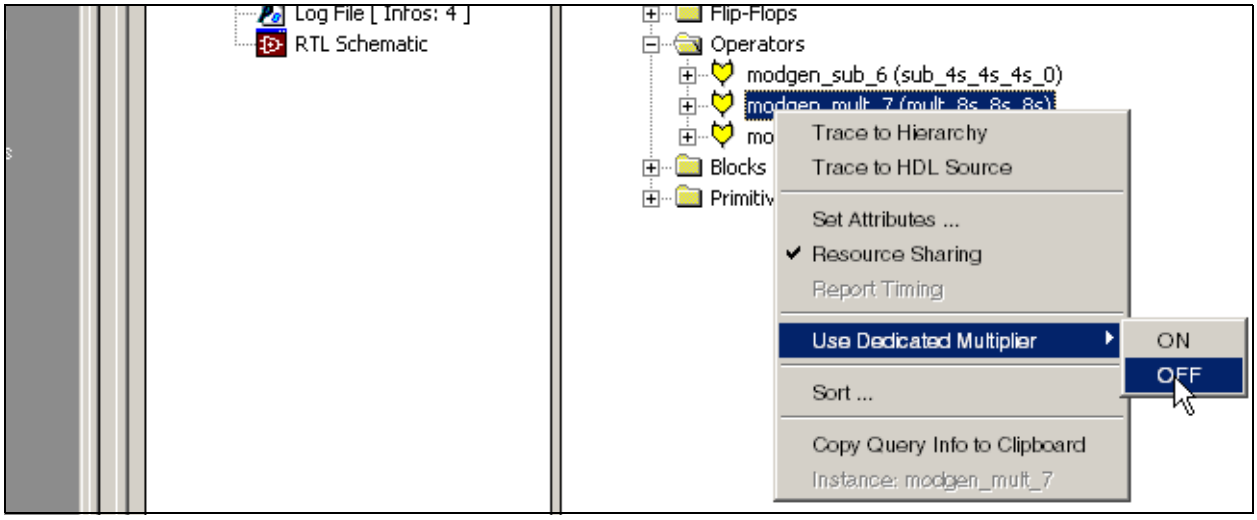
Major work has been completed to enhance the support of Virtex/Virtex-II/Virtex-II Pro RAM inferrencing and mapping. The designer can now include a RAM model that infers a variety of dual-port and tri-port RAM configurations. Refer to the Chapter 11 - Xilinx Memory Mapping in the Precision RTL Synthesis Style Guide for details and coding examples.

Virtex-II Clock Buffering Improvements

Precision RTL Synthesis now does smarter clock buffer insertion. Precision is no longer buffering low-fanout internal clocks (fanout < 100) and is limiting the use of global buffers on multiple-clock designs. The benefits are improved performance for designs with internal clocks and improved place and route run times, especially for designs with more than 8 clocks. When a clock is not globally buffered, a warning message is issued to the Transcript.

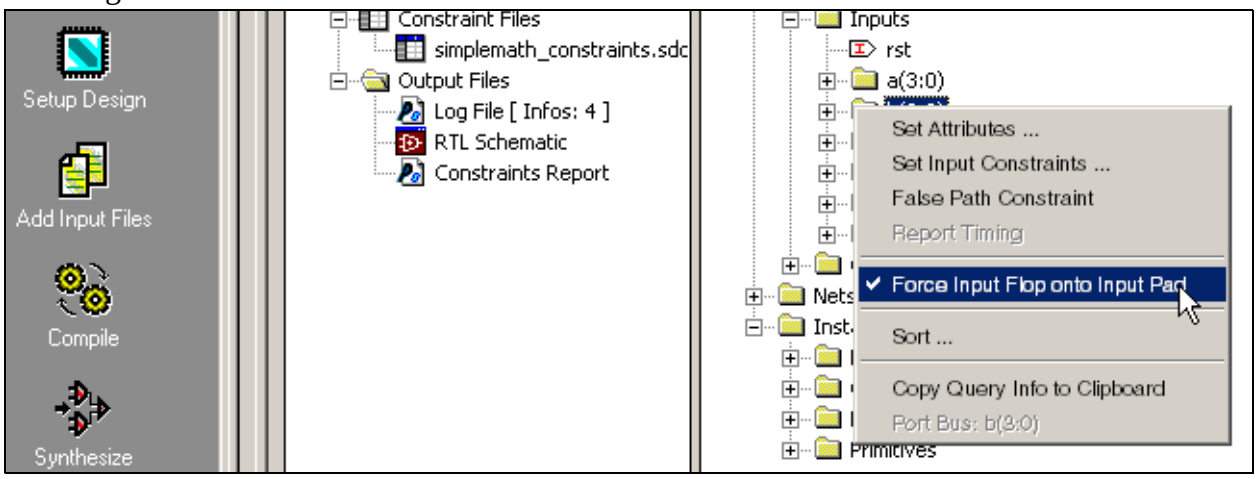
Virtex-II Multiplier Control

Virtex-II/Virtex-II Pro multiplier implementation can now be controlled by setting a constraint. After compiling your design, you can select a multiplier operator, as shown below, and select a MULT18x18 (dedicated) implementation or a MULT_AND implementation.



Virtex Timing-Driven IOB Mapping

Registers that are connected directly to ports are now automatically assigned to the IOB when timing is not impacted or when timing is improved. You can override this behavior before synthesis by right-clicking on a port in the Design Hierarchy window, as shown below, and turning the feature off.



Gated-Clock Support

Clocks are now automatically propagated through internal clock pins during the “compile” phase. This means that you can now set clock constraints for gated clocks from the primary input port. If you hover the cursor over a propagated clock pin in the Schematic Viewer, the query pop-up will display the constraint information.

New Technologies Supported

Xilinx Virtex-II Pro

Device Support for the Virtex-II Pro Family has been expanded to include the following:

New Virtex-II Pro Devices	
2VP30	fg256, ff896, ff1152
2VP70	ff1704
2VP100	ff1704
2VP125	ff1704

Xilinx Virtex-II Speed Grades

Support for Virtex-II device stepping speed grades -4s1 and -5s1 has been added.

Customer-Reported DRs Fixed

DR327436 Precision calculates the wrong slack for an Altera Stratix device.

DR327546 Precision produces an incorrect netlist on a customer design.

Known Issues

Precision is Not Supported on Solaris 8 Versions Released after Dec. 13, 2001

Precision RTL Synthesis is experiencing very long invoke times and very long run times on Sun machines with kernel version: SunOS 5.8 Generic 108528-13 December 2001 and later. This problem will be resolved in a future release of Precision. You can check the version of the Solaris Operating System by using the ‘showrev’ command.

Chapter 8
Release 2002a

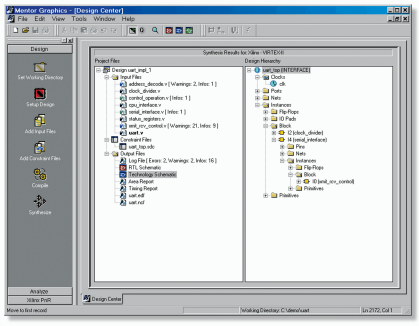
Introducing Precision RTL Synthesis

Mentor Graphics Corporation, the leader in programmable logic design solutions is pleased to introduce our newest synthesis product, Precision RTL Synthesis. Precision RTL Synthesis is a synthesis platform that maximizes the performance of both, existing programmable logic devices (CPLDs and FPGAs) and next-generation, multi-million gate field programmable system-on-chip (FPSoC) devices. Precision RTL Synthesis is a comprehensive tool suite, providing design capture in the form of VHDL and Verilog entry, advanced register-transfer-level logic synthesis, constraint-based optimization, state-of-the-art design analysis, schematic viewing and encapsulated place and route. Precision RTL Synthesis runs on Windows 98/NT/2000/XP; and UNIX Sun and HP platforms.

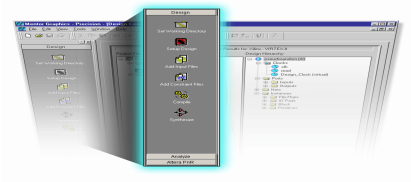
Precision RTL Synthesis Technical Overview

Precision RTL Synthesis addresses the requirements of both current and next-generation programmable logic design. The synthesis solution features an intuitive graphical user interface, a new suite of optimization algorithms (Architecture Signature Extraction™) and a state-of-the-art timing engine (PreciseTime) that delivers the industry's most accurate timing analysis.

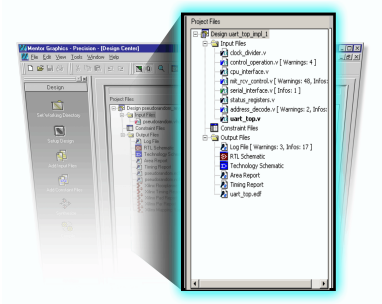
Intuitive Design Flow Eases Next-Generation Programmable Device Design



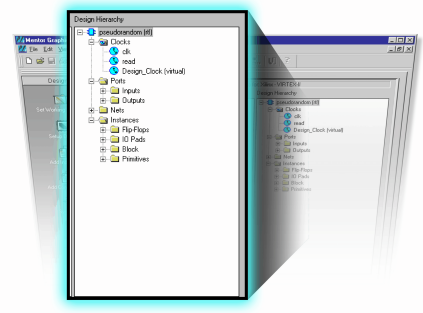
Precision RTL Synthesis accelerates time-to-productivity for both novice and experienced programmable logic designers, equipping designers with an intuitive user interface that makes achieving design goals easier. At the heart of the push-button flow is the Design Center that is driven by the design bar and provides two distinct views of the design - design view and hierarchy view.



The Design Bar guides, both novice and expert users alike, easily through the synthesis and place and route process. A progressive disclosure paradigm presents only valid next steps reducing frustration and confusion. When optimization completes, additional design bars appear to assist with design analysis and vendor place and route.

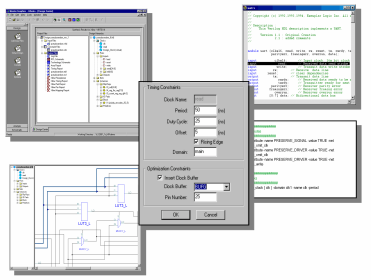


Precision's Design Center design view enables designers to perform all operations with a click of the mouse, including adding or editing design and constraint files, or viewing synthesis and place and route report files. The design view also provides revision management, enabling designers to control design iterations.



Precision's unique hierarchy view provides a view of the compiled design and is directly linked to a schematic viewer, enabling designers to find any object in the design and apply constraints directly to the object. This eliminates the need to launch additional design editors for entering constraints, which saves time, increases productivity and eliminates user frustration when working with large designs.

Precision's flexible constraint entry provides the ability to enter constraints from the design center, from the integrated schematic viewer, from any text reports as well as from user provided scripts. It also leverages industry expertise through the support of Synopsys Design Constraint (SDC) for specifying timing for the design.



Precision's User Interface Features and Benefits

Feature	Benefit
Design Center	A single user interface, the design center, provides all the control necessary to compile, constrain, optimize, analyze and place and route a design
Design Bar	Guides designers through the synthesis process without ever presenting an invalid step
Project Management	Keeps track of input and output files, provides quick access to output results and allows users to work with multiple revisions
Flexible Constraint Entry	Timing constraints can be applied throughout the system using a variety of design views
Industry Standard Constraints	Allows for easy migration between ASIC and FPGA design tools and enables designers to take advantage of most IP
Flexible Flows	Design how you want, Top Down or Bottom Up

Multiple Design Flows

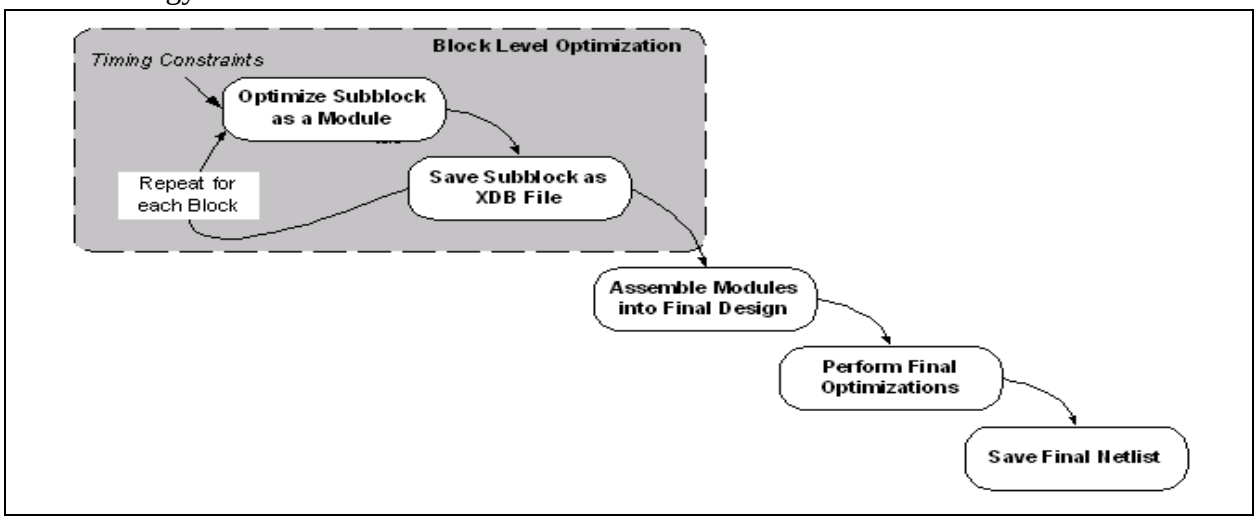
Designers require flexibility in the way they approach a design. Precision provides two basic flows, top-down and block-based. In addition, various vendor-specific advanced design flows are supported.

Top-Down Design Flow

Top-down design implies that the entire design is loaded into the synthesis environment and optimized at once. Top-down design methodologies are the easiest and generally yield the best results by allowing the synthesis tool to perform inter-module optimizations. Precision supports top-down design for the largest FPGA devices on the market today and has optimized the user interface and optimization algorithms to excel at this flow.

Block-Based Design Flow

Block-based or bottom-up design implies that the design is divided along major functional blocks and optimized in a piecemeal fashion. This design methodology is more involved but provides designers a way to manage the immense amounts of data associated with large designs. The largest FPGAs available today offer gate counts in excess of 8 million ASIC gates. Precision RTL Synthesis is unique in its comprehensive support for bottom-up design methodology for FPGAs.



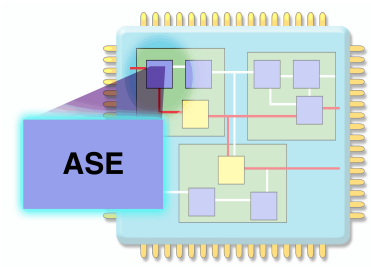
Block-Based design features and benefits are summarized in the following table:

Feature	Benefit
Optimize blocks without IO insertion	Allows sub-blocks to be optimized independent of the top-level design.
Read / write binary database	Allows a pre-optimized sub-blocks to be saved and re-read into logic synthesis.
Don't_touch attribute on blocks	Prevents re-optimization of previously sub-blocks. Preserves the integrity of block based verification efforts.
Assembly of final design from pre-optimized sub-blocks	Allows design analysis to be performed on entire design prior to place and route. Allows IO buffers to be instantiated. Allows user to perform additional optimizations if necessary.
Current Design	Allows selection of a block from within a top-level design.
Incremental Updates of blocks	Allows functional updates to be incorporated into final design with minimal re-optimization and re-place and route.

Advanced Design Flows

Precision RTL Synthesis automatically recognizes Altera's encrypted IP or the unique files associated with the Xilinx PCI core and configure the necessary synthesis and place and route settings. This automation dramatically reduces the complexity of these flows, including place and route.

A.S.E. Optimization Raises the Bar on Design Performance



Precision RTL Synthesis includes a suite of unique algorithms called Architecture Signature Extraction™ (ASE) optimization which, based on timing constraints, focuses specific optimizations on areas of the design that likely hinder overall performance, such as finite state machines (FSMs), cross-hierarchical paths, or paths with excessive combinational logic. ASE optimization uses an automated, heuristic approach to deliver smaller designs that achieve project requirements in less time by reducing the manual process of isolating and correcting problem areas in a design. ASE optimization performs advanced technique tasks such as Look-up Table (LUT) merging, logic tunneling, register re-timing and timing-driven I/O block (IOB) mapping to reach the target performance without the need for iterative manual user intervention.

Precision's advanced optimization technology breaks down performance limiting design barriers such as register, hierarchy and operator boundaries to provide you with the smallest and fastest design possible.

PreciseTime Drives Performance and Provides Rapid Design Analysis

Precision RTL Synthesis includes PreciseTime; an incremental timing engine that provides advanced functionality previously found only in stand-alone static timing analysis tools. PreciseTime's advanced analysis includes the following:

- RTL Analysis that reports warning and errors in your RTL and traces them back to the source code.
- Graphical Analysis so that you can view your design in RTL
- Constraint Analysis to ensure your design is properly constrained
- Area Analysis to ensure your design fits in the desired device

- Incremental Timing Analysis that reports timing on any pin or port in the design
- Cross-Clock Domain Analysis to ensure that there are no meta-stable clocks
- Mapped schematics that can be filtered to show only critical path fragments
- Cross-probing between schematics, reports and source code

Design Analysis Features and Benefits

Feature	Benefit
Language Analysis	VHDL and Verilog design templates. Cross-probing from error messages back to source code.
Constraint Analysis	Verifies that a design is fully constrained. Insures that no critical paths are overlooked.
Clock Domain Analysis	Ensures that asynchronous clocks are truly asynchronous. Eliminates problems from meta-stable clocks.
Critical Path Schematic Fragment	Lets designers focus on a small view of important logic in their designs.
Fan-in Fan-out Fragment Viewing	Allows designers to isolate critical logic for viewing all the logic to or from a particular node. Powerful viewer for viewing clocks or the logical source of a node.
Timing Violations Report	Constraints without a violation are not displayed. Provides a list of constraints that have a timing violation.
Incremental Timing Analysis	Provides fast “what-if” analysis of design timing. Change constraints and get new timing information immediately.
Generate Timing Reports from Schematics	Allows efficient starting point for timing reports. Gives designers a deep knowledge of their design timing. If place and route shows a different path, you can easily display the same logic.
Timing Report to Schematic Cross-highlighting	Quickly reference nets or instances in a timing report to the schematic. Once located, fan-in and fan-out schematics can be quickly located.

Devices Supported

This release of Precision RTL Synthesis supports the following Altera and Xilinx families.

Altera Devices Supported

Altera Device Families Supported
Stratix
Excalibur ARM
Mercury
APEX II
APEX 20K/20KE/20KC
FLEX 6000/8000/10K
ACEX
MAX

Xilinx Devices Supported

Xilinx Device Families Supported
Virtex-II/Virtex-II Pro
Virtex/Virtex-E
Spartan-II/Spartan-IIE
XC4000/XC5200

Additional Device Support

Additional Vendor Devices will be supported in upcoming releases.

For a complete list of devices currently supported, refer to Chapter 4 in the Precision Synthesis Reference Manual.

Known Issues

Precision is Not Supported on Solaris 8 Versions Released after Dec. 13, 2001

Precision RTL Synthesis is experiencing very long invoke times and very long run times on Sun machines with kernel version: SunOS 5.8 Generic 108528-13 December 2001 and later. This problem will be resolved in a future release of Precision. You can check the version of the Solaris Operating System by using the 'showrev' command.

How You Can Learn More...

Context-Sensitive Help

Precision RTL Synthesis provides context-sensitive help throughout the GUI. You can press **F1** to open a context-sensitive help or press the HELP button. The GUI window must be selected first to be in current focus when using F1. (Note: F1 is not available for UNIX.)

You can also view frames of help text and graphics by moving your cursor to the Help pulldown menu and selecting: **Help > Help Contents...** You can expand the Table of Contents and select from a variety of topics or do a full index search for keywords.

Product Manuals

All Precision RTL Synthesis product manuals are available for on-screen viewing and printing with the Adobe Acrobat Reader after Precision RTL Synthesis and the Adobe Acrobat Reader are installed. You can view the manuals by selecting the following pulldown menu from the Main menu: **Help > Open Manuals Bookcase**

The PDF manuals and the Manuals Bookcase also contain HyperText links that guide you to related vendor documentation on the Web, provided your web browser is operational and properly configured.

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