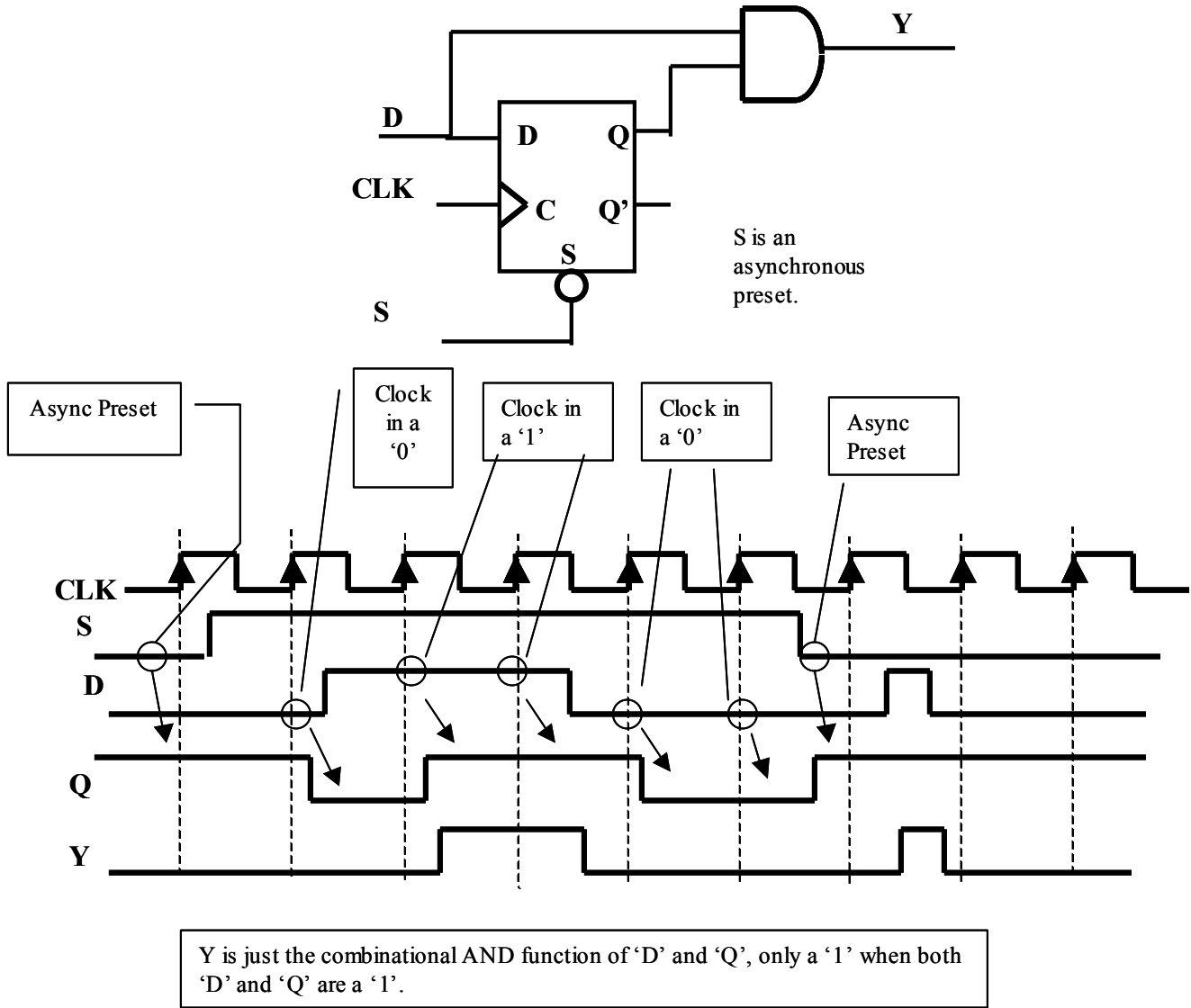
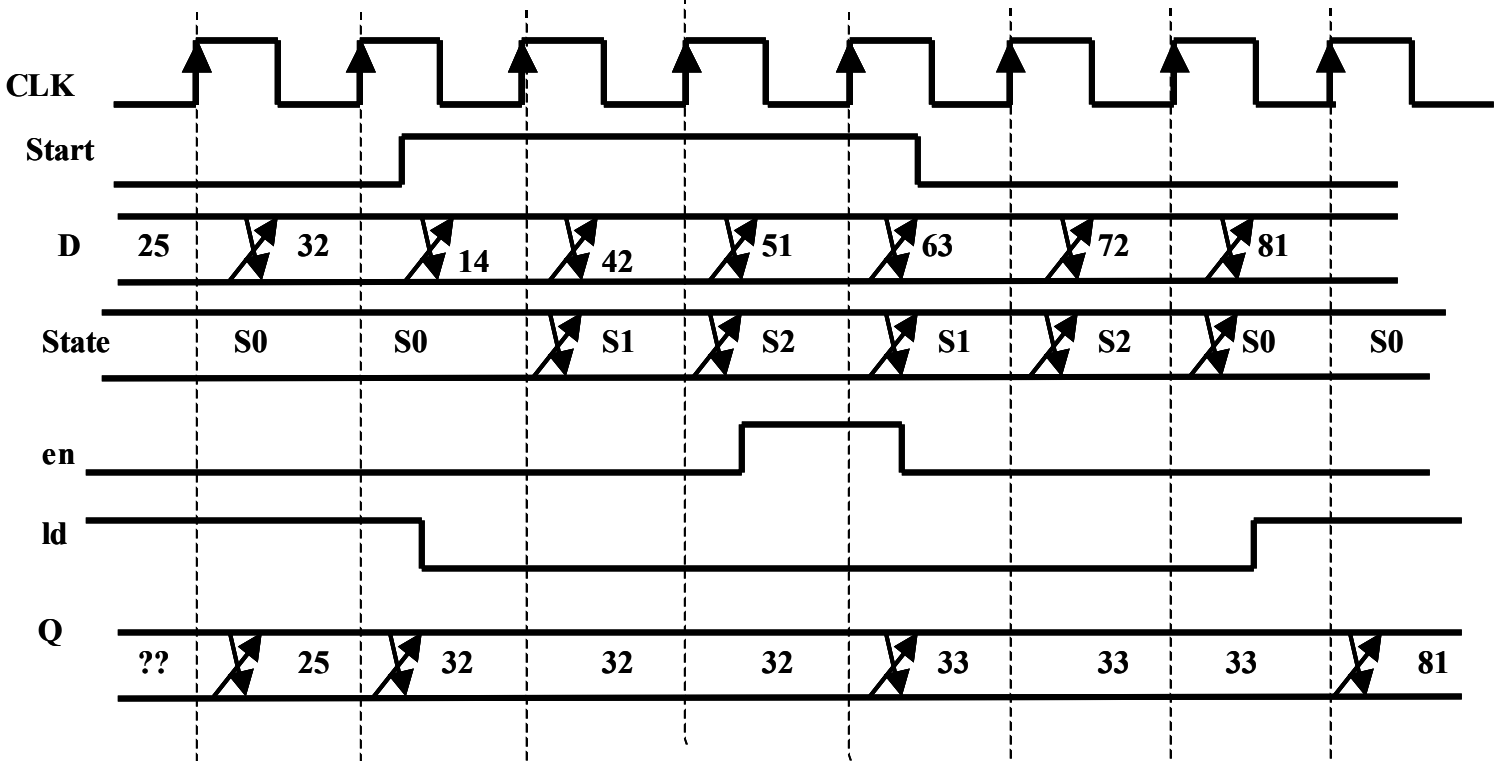
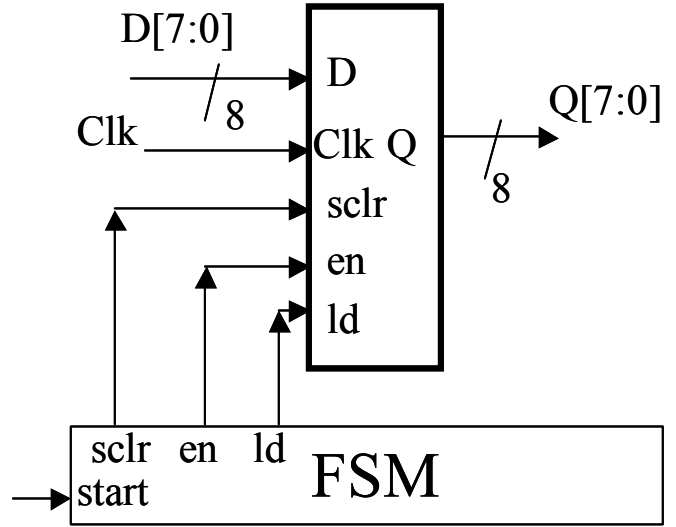
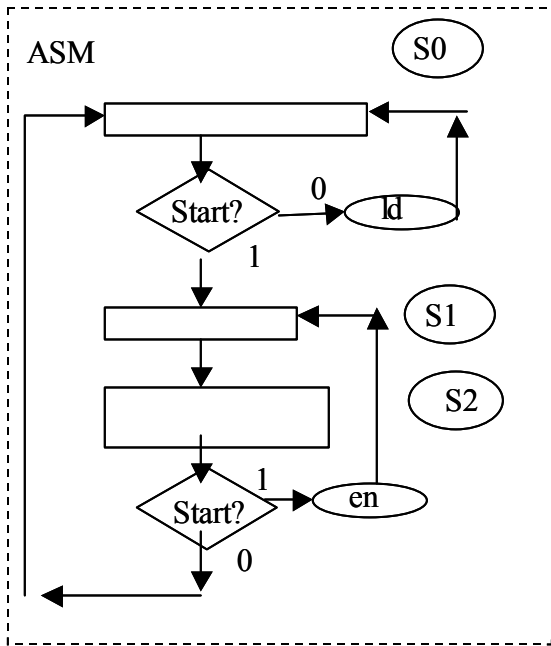


For any partial credit, you must show your work.

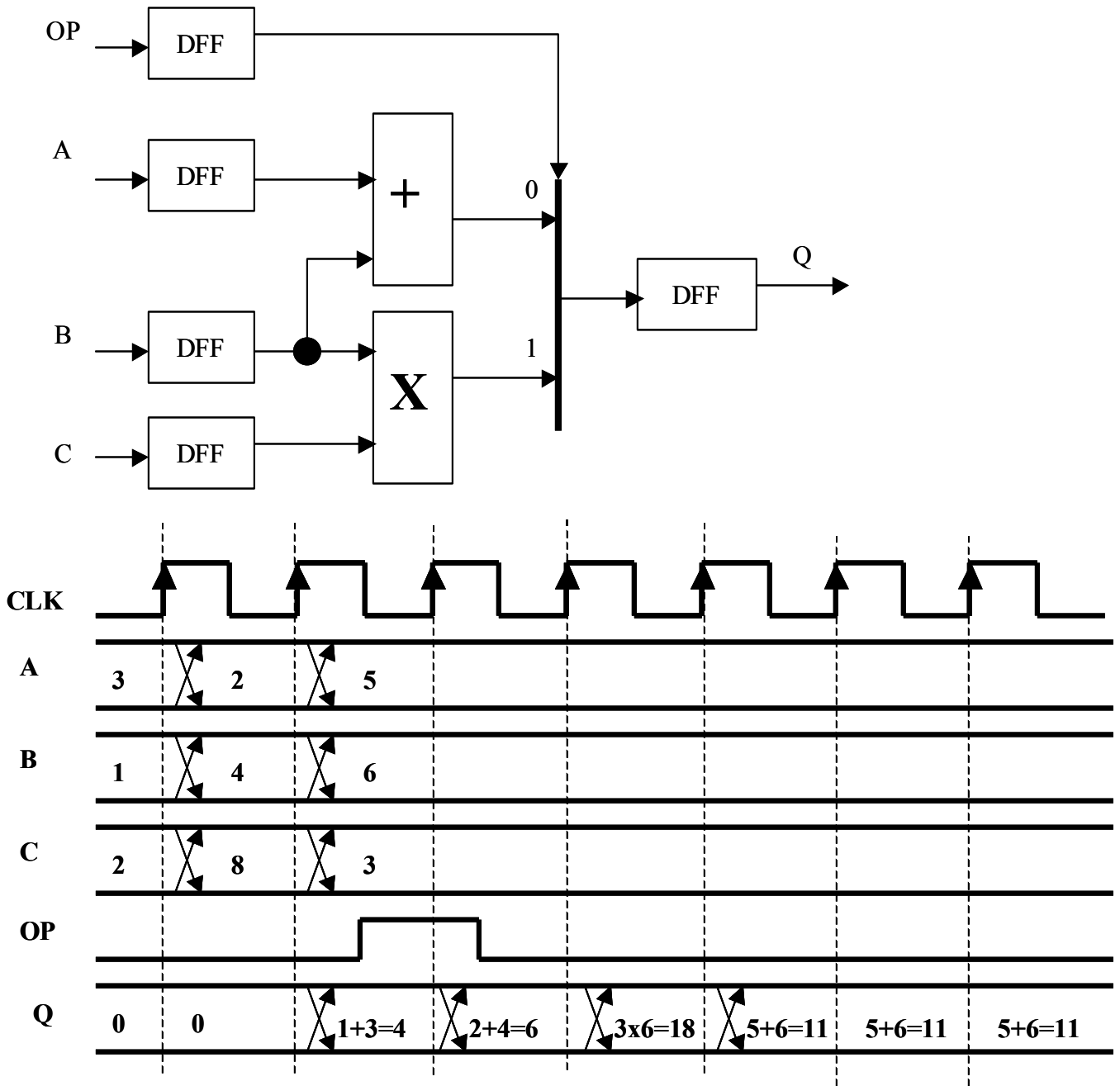
1. (15 pts) On the diagram below, complete the timing diagram for the Y output for all clock cycles.



2. (20 pts) On the waveforms below, complete the waveforms for State, ld, en, and Q. The FSM is controlling an UP counter, LD has precedence over EN.



3. (15 pts) For the datapath below, fill in the value for the Q output.



4. (15 pts) For the datapath below, and the timings shown, do the following (for all timing calculations, do not just give me a number; you must show me how you calculate the number or you will not get any credit).

Timings for datapath: Adder delay: Max(10 ns), Min (4 ns)  
 Multiplier delay: Max (18 ns), Min (10 ns)  
 Mux delay: 4 ns (Max = Min delay)  
 C2Q of DFF: 3 ns (Max = Min delay)  
 Tsetup of DFF: 2 ns (Max setup)  
 Thold of DFF: 1 ns (Min hold time)

- a. Compute the maximum register-to-register delay.

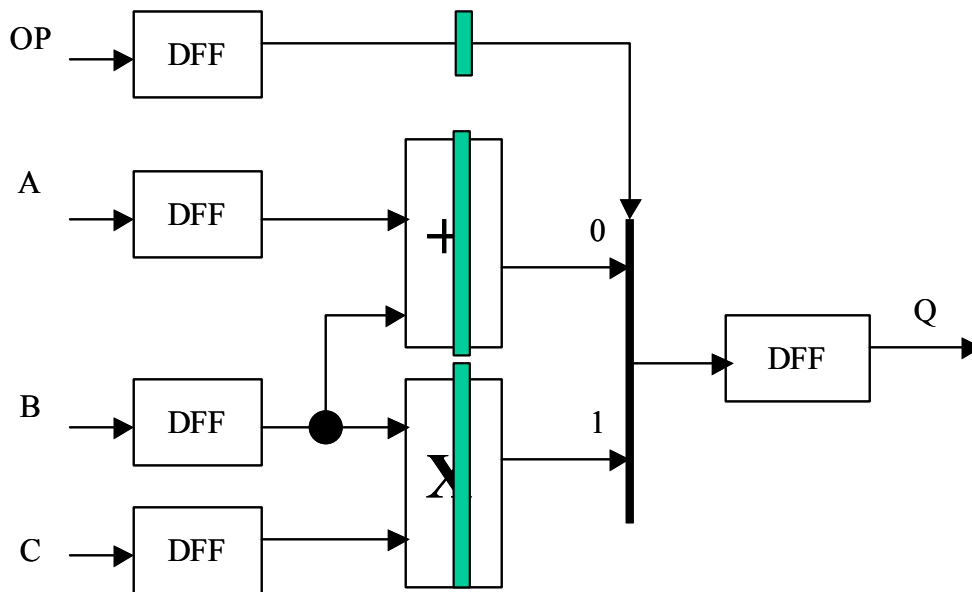
$$T_{cq} + Mult(Max) + Mux(max) + T_{su} = 3 + 18 + 4 + 2 = 27 \text{ ns}$$

- b. Show where one level of pipelining could be inserted where it have the most speed benefit. Place pipeline registers on all paths that require them to maintain data alignment.

See diagram.

- c. Compute the new maximum register-to-register delay for your pipelined design.

$$T_{cq} + 1/2Mult(Max) + Mux(max) + T_{su} = 3 + 9 + 4 + 2 = 18 \text{ ns}$$



5. (15 pts) For the datapath below, and the timings shown, do the following (for all timing calculations, do not just give me a number; you must show me how you calculate the number or you will not get any credit).

Timings for datapath: Adder delay: Max(10 ns), Min (4 ns)  
Multiplier delay: Max (18 ns), Min (10 ns)  
Mux delay: 4 ns (Max = Min delay)  
C2Q of DFF: 3 ns (Max = Min delay)  
Tsetup of DFF: 2 ns (Max setup)  
Thold of DFF: 1 ns (Min hold time)

None-clock Input buffer delay (Max = 2 ns, Min = 1 ns)  
Clock input buffer delay (Max = 4 ns, Min = 2 ns).

- a. Compute the external Setup time for input 'B'.

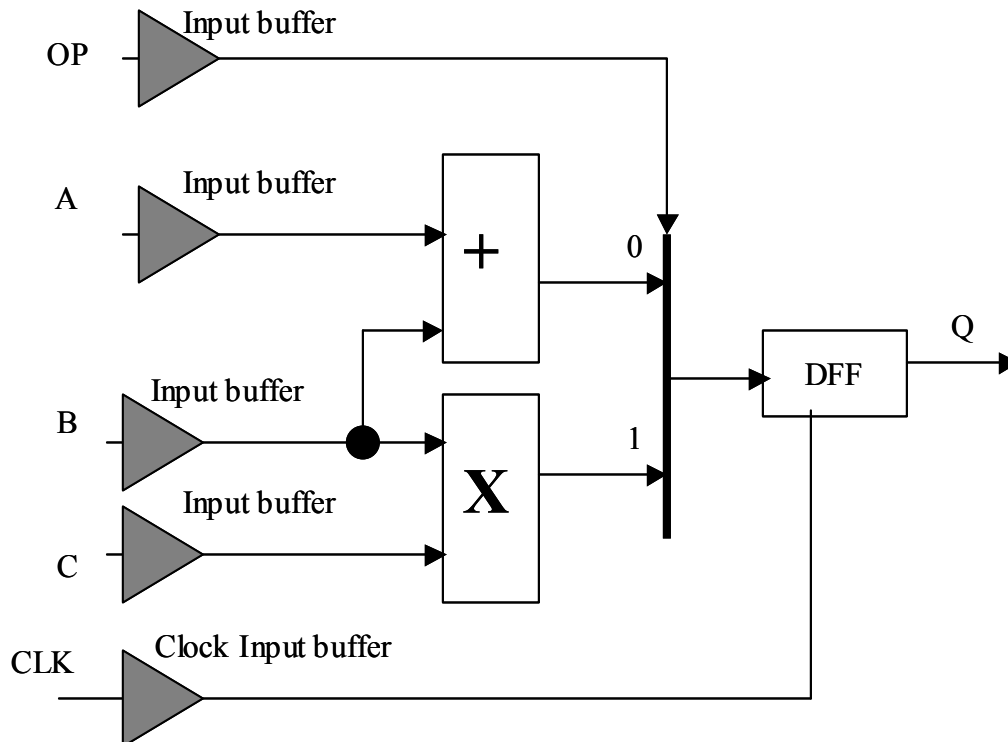
$$\begin{aligned} T_{su} (ext) &= T_{su} + \text{Max Tpd for B} - \text{Min Tpd for Clock} \\ &= T_{su} + (\text{Non-clock buffer Max} + \text{Mult Max} + \text{Mux Max}) - (\text{clock buffer min}) \\ &= 2 + (2 + 18 + 4) - 2 = 24 \text{ ns} \end{aligned}$$

- b. Compute the external hold time for input 'B'.

$$\begin{aligned} T_{hd} (ext) &= T_{hd} + \text{Max Tpd for clock} - \text{Min Tpd for B} \\ &= T_{hd} + (\text{clock buffer max}) - (\text{non-clock buffer min} + \text{Adder min} + \text{mux min}) \\ &= 1 + (4) - (1 + 4 + 4) = -4 \text{ ns} \end{aligned}$$

- c. Compute the maximum Clock-to-Out time for Q.

$$\text{Clock to Out} = \text{Clock buffer max} + T_{cq} = 4 + 3 = 7 \text{ ns.}$$



6. (4 pts) What is the truth table for the following VHDL? (two inputs are A, B. The output is Y).

```
process (a, b)
begin
  Y <= '0';
  if (a = '1') then Y <= '1';
  elsif (b = '0') then Y <= '1';
  end if;
end process;
```

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

7. (4 pts) One function of a Phased Locked Loop (or Delay Locked Loop) is to do clock frequency multiplication and division. What is another function of a PLL (or DLL)?

*Align internal and external clock edges – removes clock input buffer delay.*

8. (4 pts) What the value of 12H + 70H in signed saturated addition mode?

Binary addition: 12H + 70H = 82H , positive+positive = negative, so overflow.  
Clamp to maximum positive value = **7FH**.

9. (4 pts) What the value of 12H + 70H in unsigned saturated addition mode?

Binary addition: 12H + 70H = 82H , no carry out, so final result = **82H**.

10. (4 pts) What is the binary value of 3.25 in 4.4 fixed point format?

3.25 = 0011.0100 = 00110100 = 34H