SOPC WORLD 2002

The MathWorks

MathWorks Integrated Design Solution

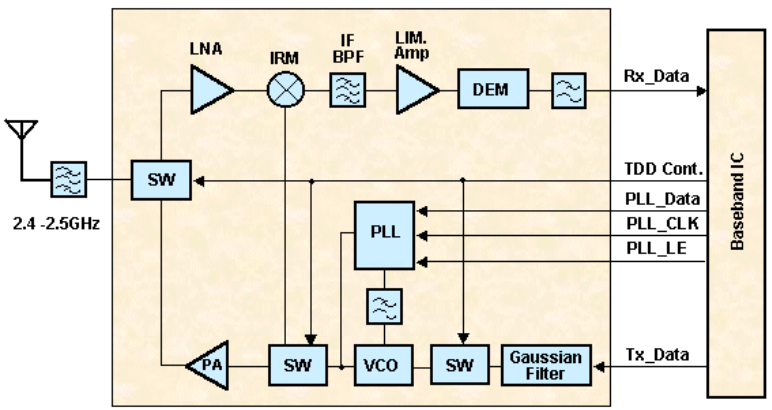
ALTERA.

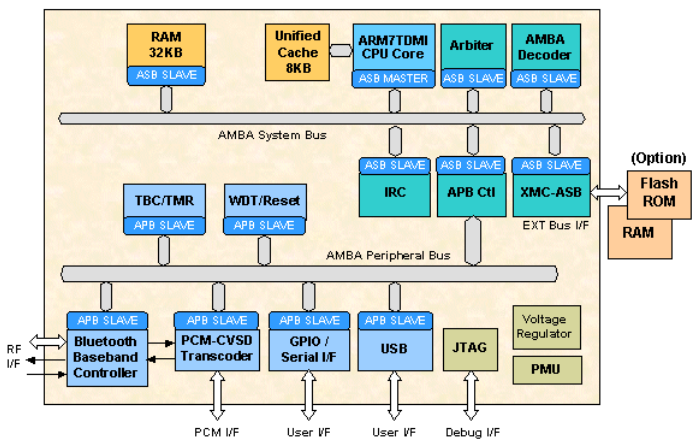
The MathWorks at a Glance

- Founded in 1984, privately held
- Headquarters in Natick, Massachusetts (near Boston)
- European offices in the UK, France, Germany, Switzerland, Italy, Spain, and Benelux region
- Over 1000 employees, including 1/3 in product development
- More than 500,000 users in 100 countries, on all seven continents!

Today's System and IC Design Challenges

- Hardware: RF/Analog, Digital IC, FPGA
- Software: DSP, MAC, Control, Use interface
- Moving partitioning boundaries
  - Analog ↔ Digital IC ↔ FPGA ↔ DSP S/W ↔ Micro controller S/W
- Implementation specific tools lock your IP into one target type
  - Spice, HDL, ASM , C/C++

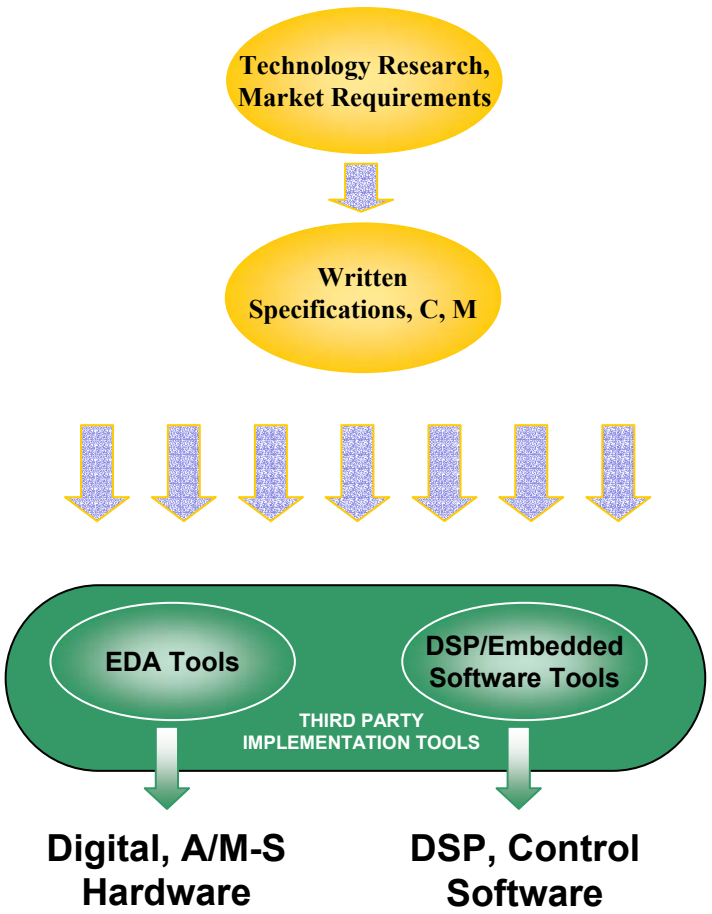




Today's Business and Organization Challenges

- Time-to-market pressure
  - A few months delay has huge revenue impact
- Team integration
  - Analog/Mixed-Signal, Digital hardware, DSP S/W, Control S/W teams
  - All speak a different language and communicate via written documents
- Increasing ASIC mask costs

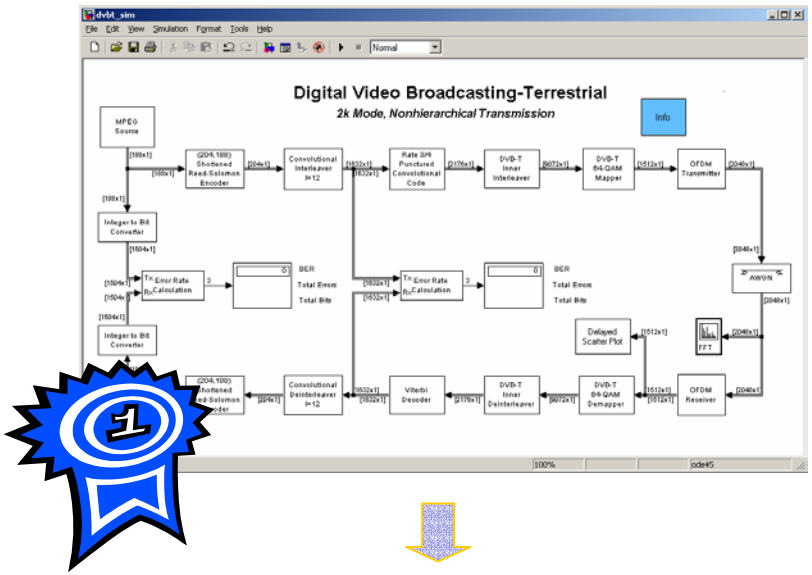
Traditional Flow: Little or No Early Simulation



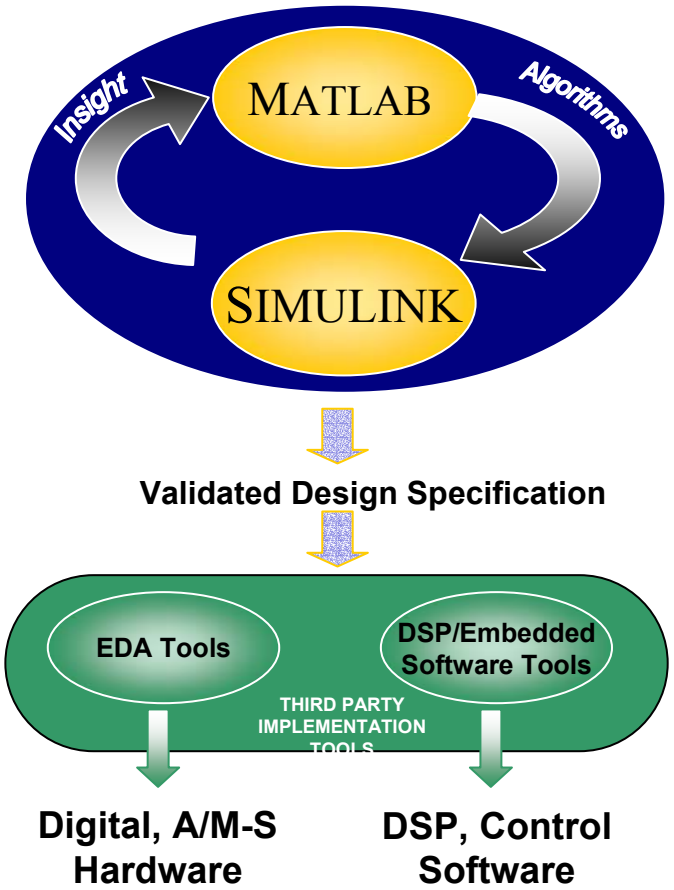
- Technology research and market requirements
- Systems engineering
- Partition into components create written specifications for teams
- Minimal or no simulation. C, M
- Design failure risk high. Flaws detected late, during circuit level, RTL or C/ASM code design
- Risk of time-to-market delays

What if You Could…?

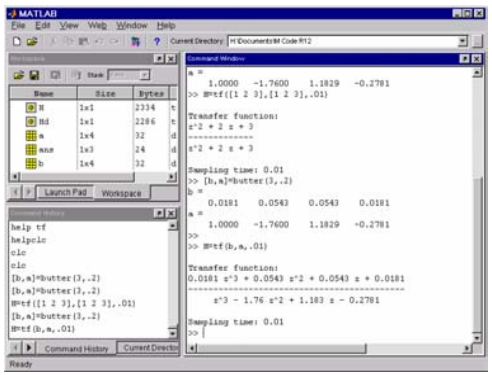
- Build a model of a complete system in minutes or days
- Simulate the behavior of the whole system before starting low-level design work?
  - Analog, digital and control together
  - Test for design flaws early
  - Trade-off architectures and parameter in minutes find best design
- Communicate your ideas and share with other teams?
- Keep your IP in an implementation neutral tool as long as possible?
- Only start development with a validated, fully tested design?



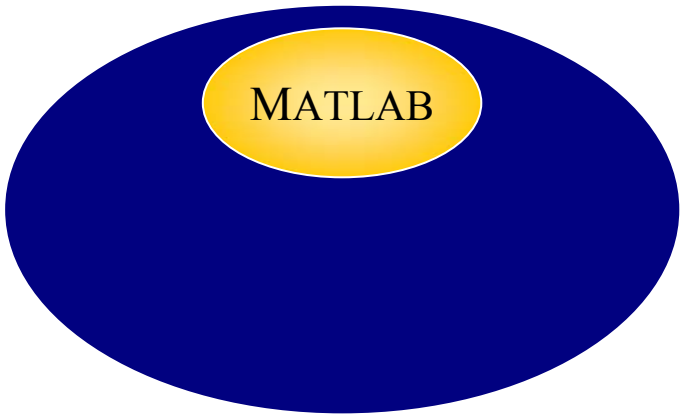
The MathWorks System-Level Solution

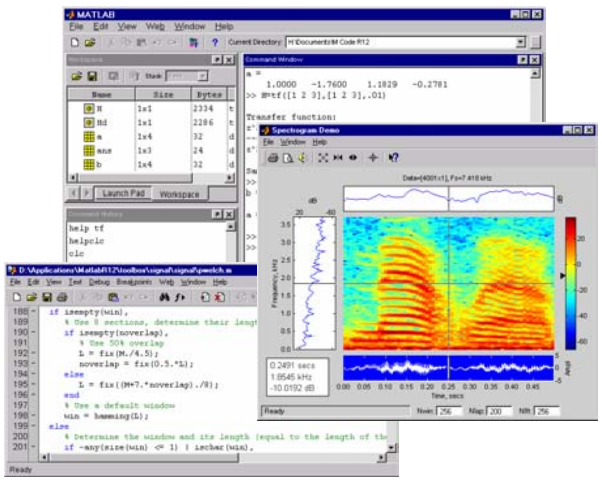


- MATLAB and Simulink
- Before circuit level, RTL or C/ASM code design
- Create a validated reference design



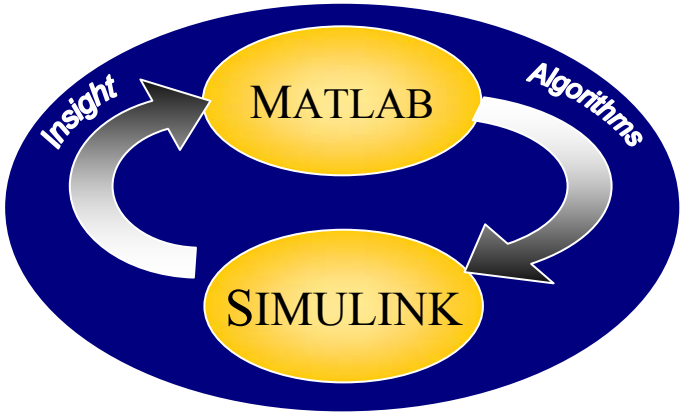
MATLAB

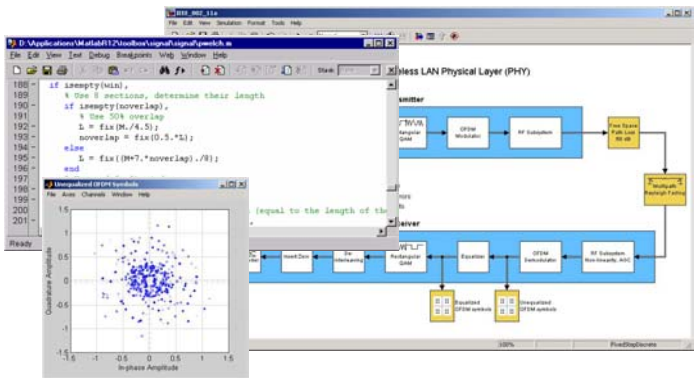




- Research new technology
- Perform mathematical modeling
- Development algorithms
- Acquire, visualize and analyze data

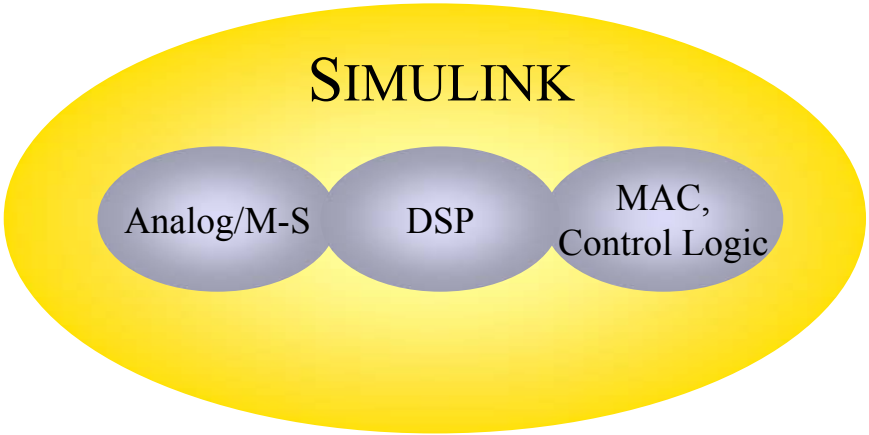
Simulink

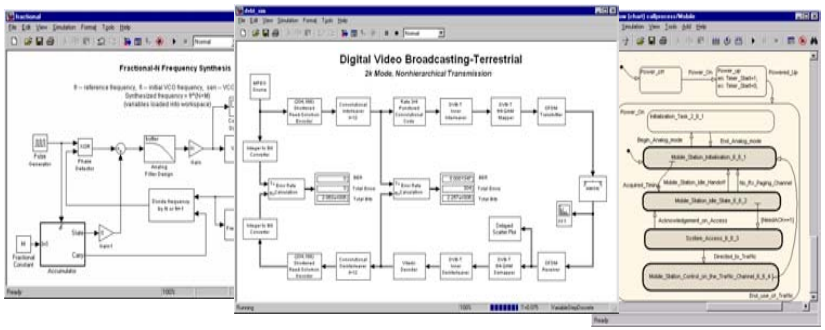




- Graphically design architecture and simulate behavior of whole system. Bit-true cycle accurate.
- From libraries of pre-built blocks
- Import C or MATLAB Code
- Test, optimize, explore parameter and architecture trade-offs

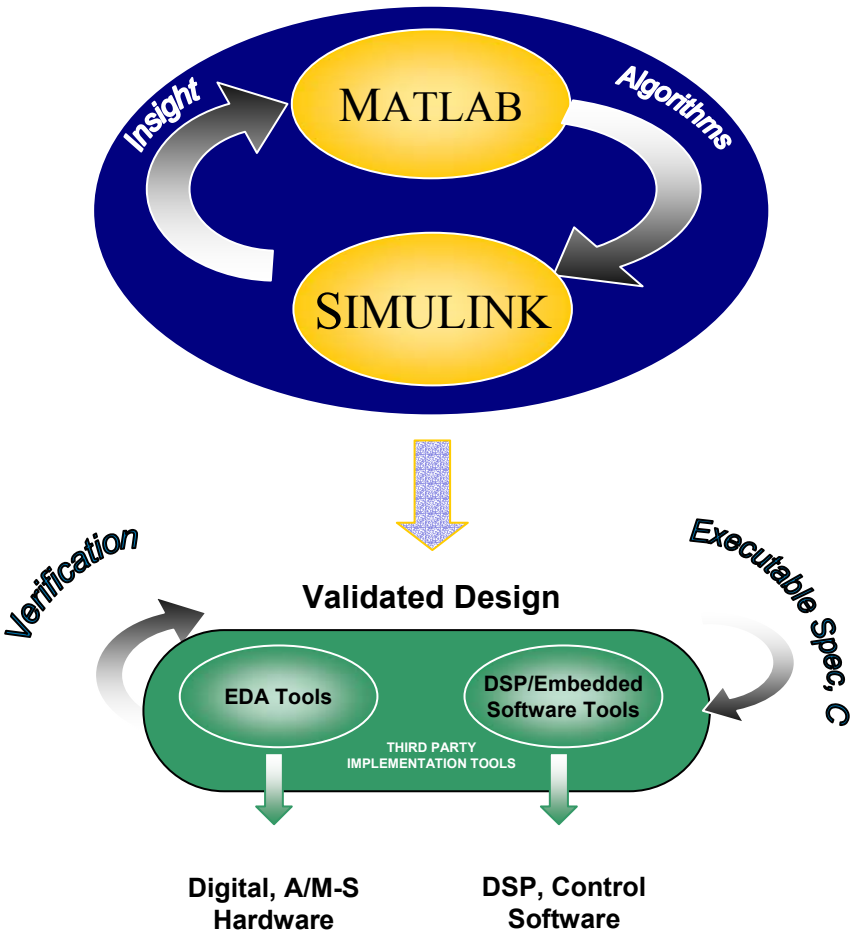
Model Different Components



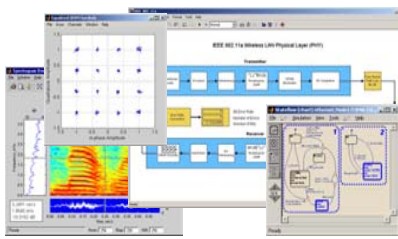


- Analog/Mixed-Signal
  - PLLs, data converters
  - Continuous time, variable-step ODE solvers
- DSP Baseband
  - Discrete time, fast frame-based processing. Bit-true cycle accurate.
- MAC layer/Data Link Layer
  - Simple protocols, acknowledgement schemes
  - Reactive or event driven state machines
  - With Stateflow

Use a Validated Design



- Create validated design
- Use as reference or executable specification to test low-level designs against
- Provide clear specifications
- Detect design flaws early
- Reduce design risk and time-to-market



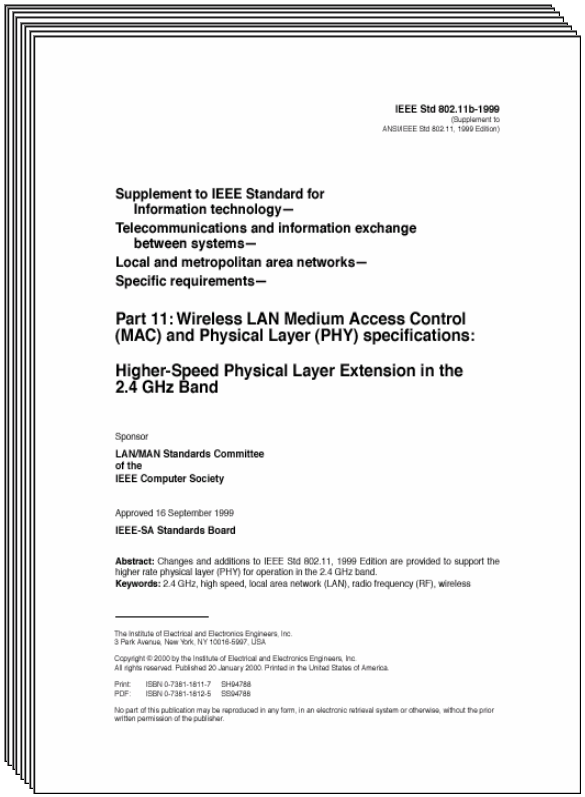
Motorola's Wireless Subscriber Systems Group

- Challenge
  - Mixed-signal Phase-Locked Loop (PLL) design
  - Cycle-to-cycle jitter and loop locking sensitivity
  - SPICE/Verilog
  - 100 μsecs: 2 hours
- Solution
  - Simulink
  - Faster development time and simulation time
  - 100 μsecs : 2.5 mins
  - Sub-picosecond resolution

> *"The Simulink models exceeded our project specifications for required simulation speed. Accurate simulations can now be measured in minutes rather than hours or days."*
>
> Yuan Yuan, Motorola

PHY Design Case Study: IEEE 802.11b

- IEEE Standard Document
  - 600 pages (11 + b appendix)
  - 4 modes (1, 2, 5.5 and 11Mbps)
- Components
  - Framing and CRC
  - Long/short preamble and sync
  - Modulation and spreading
  - Filtering
  - Channel number selection (1-11)
  - RF subsystems, Tx power, mask, power-on ramp



IEEE Std 802.11b-1999
(Supplement to
ANSI/IEEE Std 802.11, 1999 Edition)

Supplement to IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements—

Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications:

Higher-Speed Physical Layer Extension in the 2.4 GHz Band

Sponsor

LAN/MAN Standards Committee of the IEEE Computer Society

Approved 16 September 1999

IEEE-SA Standards Board

Abstract: Changes and additions to IEEE Std 802.11, 1999 Edition are provided to support the higher rate physical layer (PHY) for operation in the 2.4 GHz band.
Keywords: 2.4 GHz, high speed, local area network (LAN), radio frequency (RF), wireless

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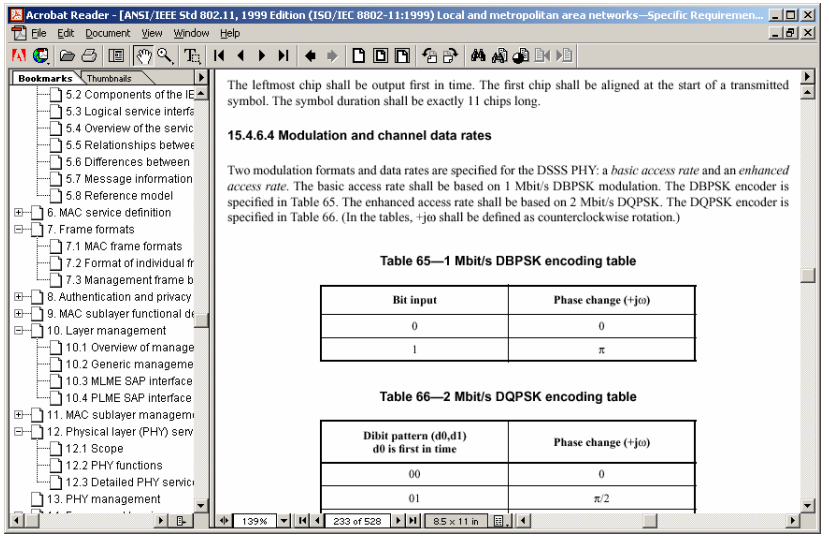
1Mbps Mode

- Modulation
  - DBPSK
- Spread
  - 11 chips Barker sequence per symbol
- Pulse shaping
  - 4/8 samples per chip
  - Root raised cosine
- Channel
  - AWGN



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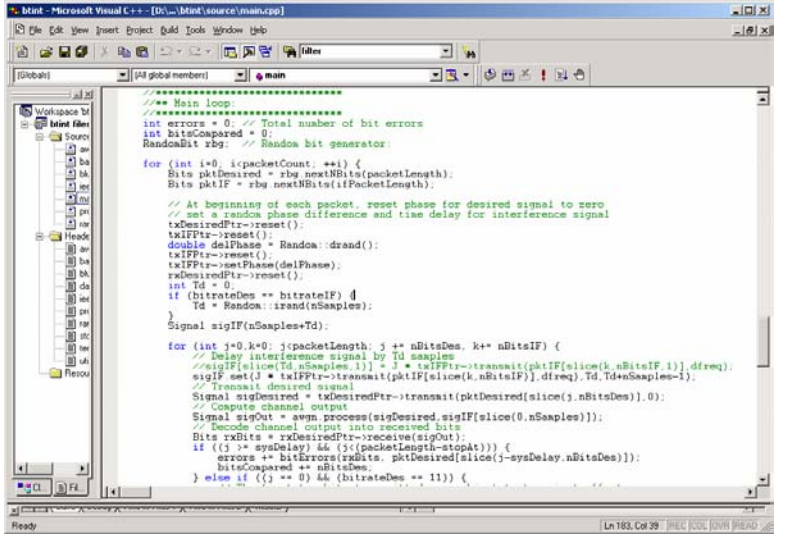
C/C++



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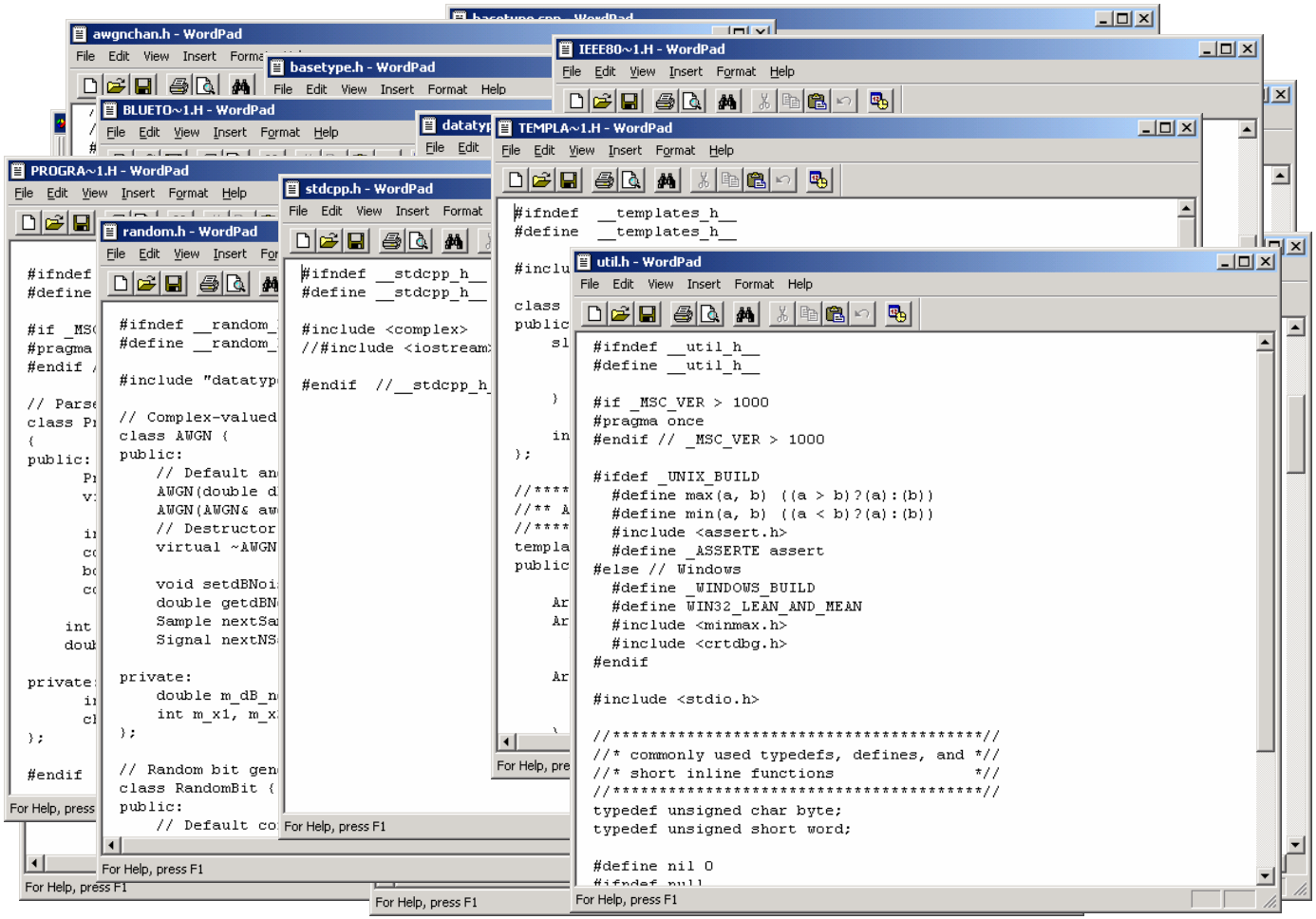
NIST 802.11b and Bluetooth C/C++ Code

- w3.antd.nist.gov/wctg/bluetooth/btint.html
- Bluetooth and 802.11b
- 802.11b
  - Random bits
  - 1 or 11Mbps modulation and spreading
  - Filtering
- Bluetooth
  - Random bits
  - Modulation
  - Filtering

C/C++ Code: 17 Files, 1500-2000 lines



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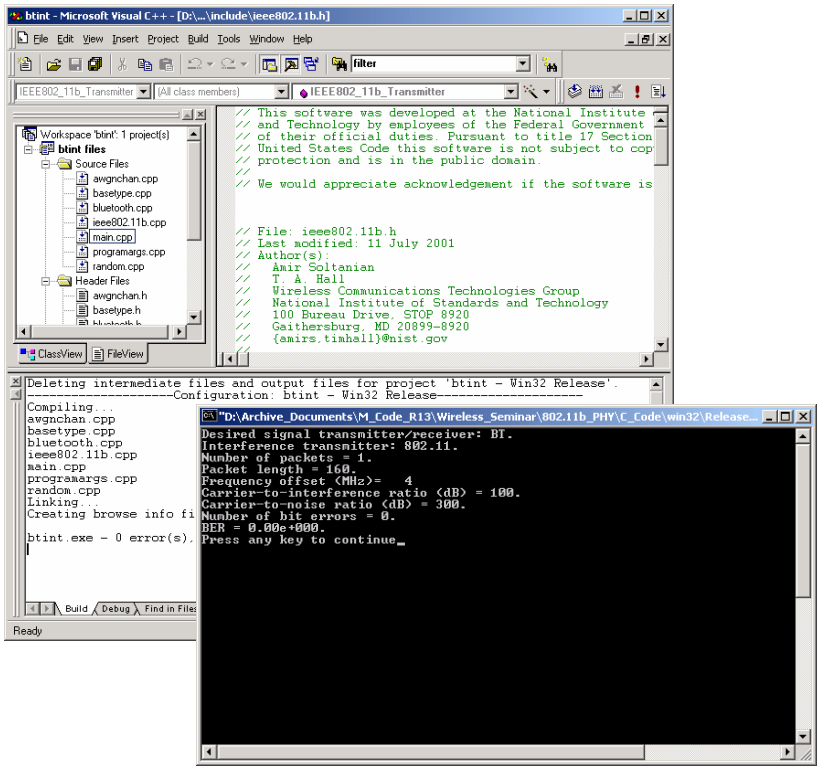
C/C++ Code: Build, Run, Debug, and Change

- Build and run
  - Bug: File I/O
- Speed
  - 7 secs for 100 packets
- Time to create
  - 400 days @ 5 lines/day
  - 40 days @ 50 lines/day
- Removing Bluetooth
  - Difficult. Many implicit dependencies

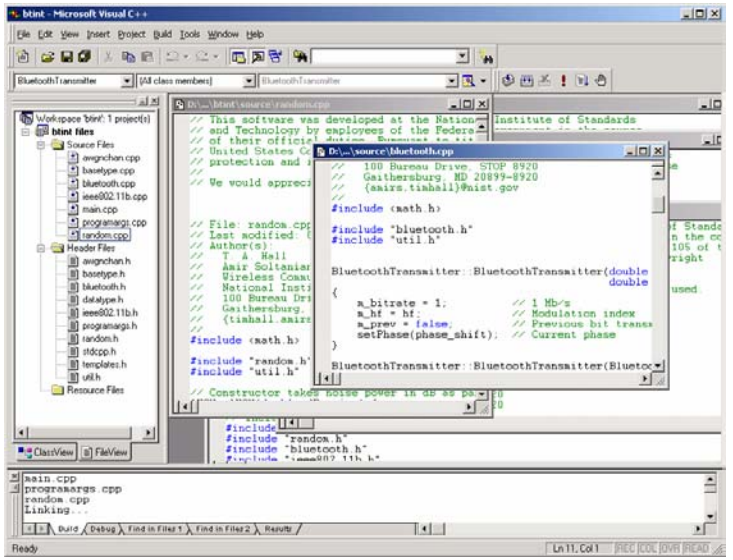



```
D:\>btint -c 100 -d 802.11 -i BT -EbNo 6
```

S/W Demonstration

C/C++ Pros and Cons

- Pros
  - Ubiquitous
  - Fast to execute
  - Data type options
- Cons
  - No canned DSP/Comm functions
  - Can't visualize signals
  - Too low-level, lots housekeeping
  - Error prone design entry, implicit interdependencies
  - Slow to iterate, debug and make changes



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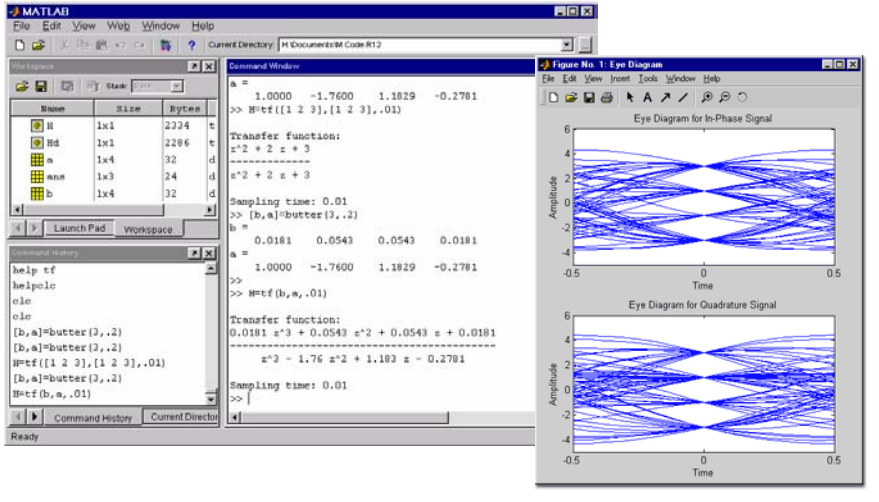
MATLAB



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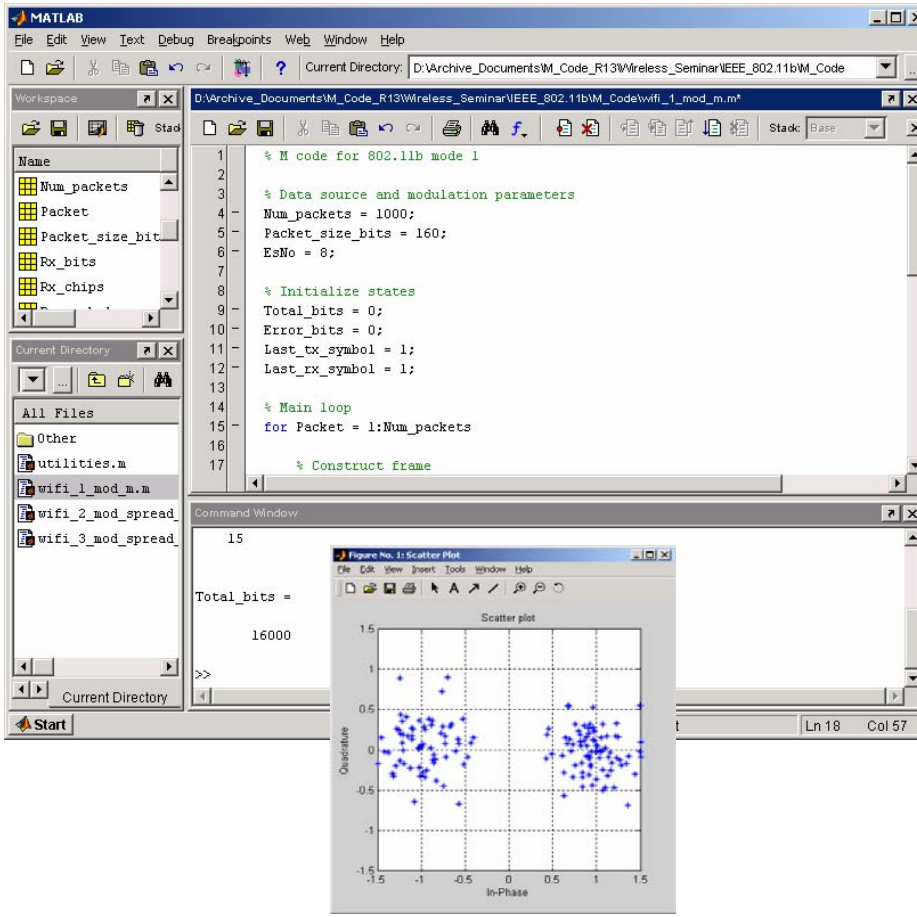
802.11b: M Code

- Using MATLAB
  - Generating bits
  - Symbols and noise
  - `scatterplot(Rx_symbols)`
- 802.11 Tx lines of code
  - One single file 52 lines
  - Modulation (3 lines)
  - Spreading (1 line)
- Speed
  - 2 secs for 100 packets
- Find the bug



S/W Demonstration: Build and show

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MATLAB Vs C/C++: Spreading and Upsampling

- **C Code**

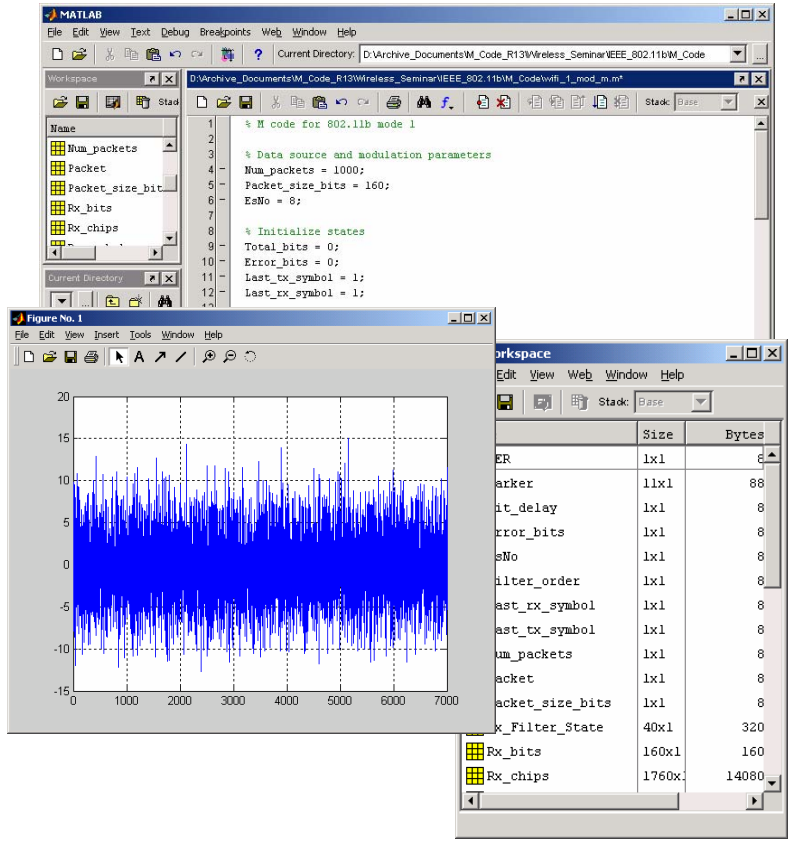
```
Bits spread=addChips(diffOut[slice(i,1)]);

Bits
IEEE802_11b_Transmitter::addChips(const Bits& input) {
    Bits spreadOut(input.size()*Ns,false);
    for (int i=0;i<input.size();++i){
        for(int j=0; j<11; ++j) {
            spreadOut[i*Ns+4*j]= m_chip[j]^input[i];
        }
    }
   return spreadOut;
}
```

- **M Code**

```
Tx_chips=reshape(Barker*Tx_symbols',[],1);
Tx_samples(1:Samples_per_chip:end)=Tx_chips;
```

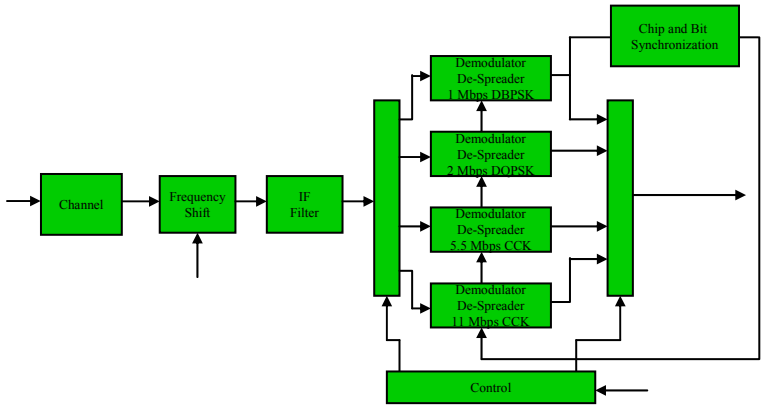
MATLAB Pros and Cons

- Pros
  - Interactive
  - Easy signal visualization
  - Canned common functions
  - Faster development
- Cons
  - Limited data types
  - Limited low-level control
  - Less memory efficient
  - Slower to execute for scalars, loops before R13



Limitations of C and M for System Design

- No architecture information
  - Can only model a pipeline
  - Can't describe a real system
- No timing information
  - Can only model uniform Fs
  - Difficult to model delays
  - Must manually handle state
  - Can't model A/M-S
  - Difficult to model Rx algorithms



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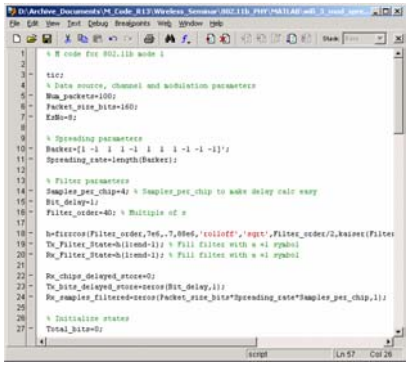

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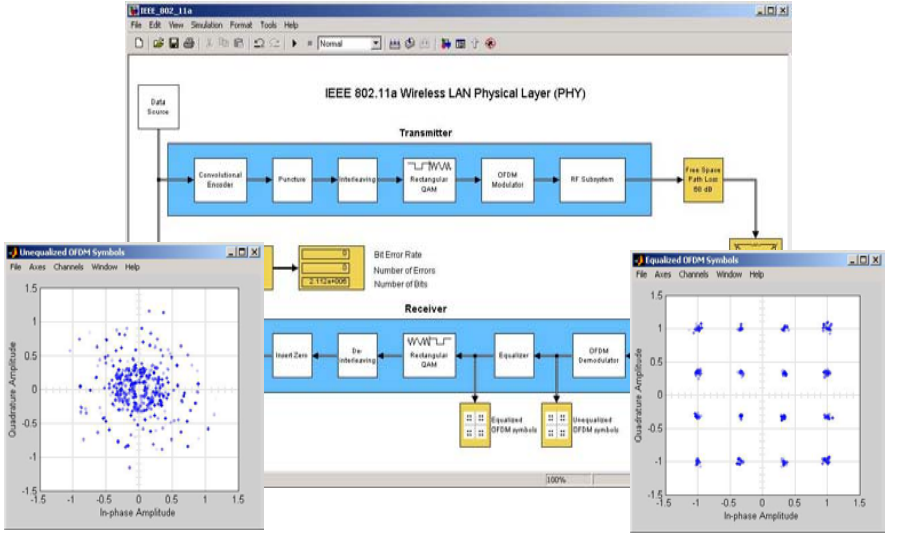
Simulink



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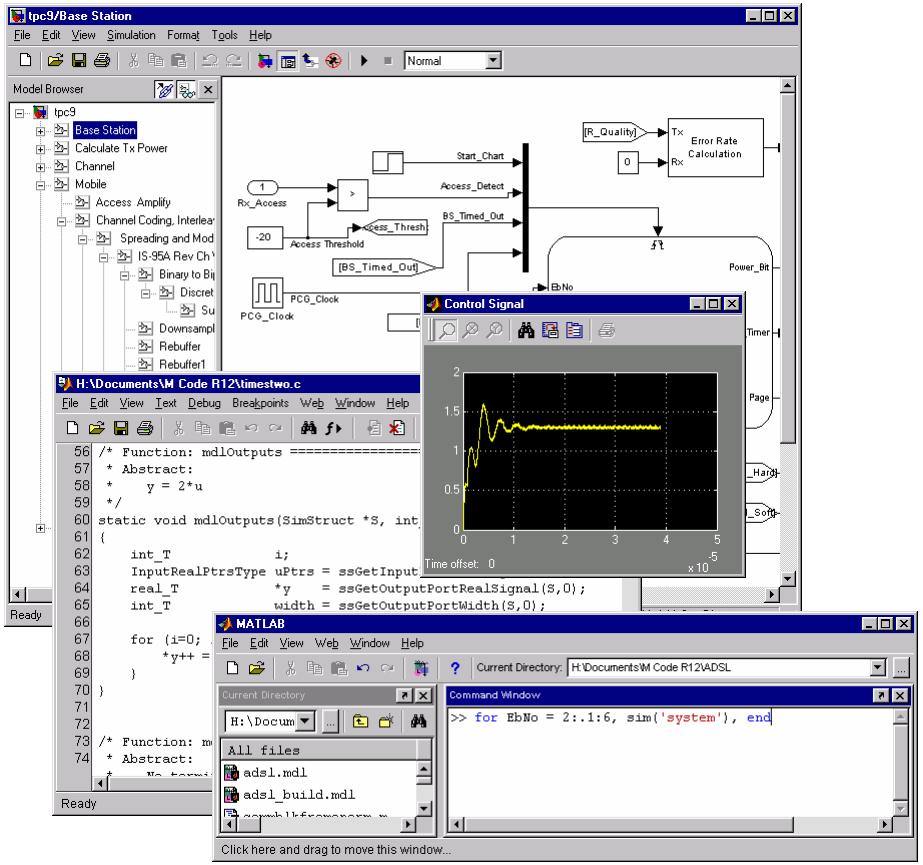
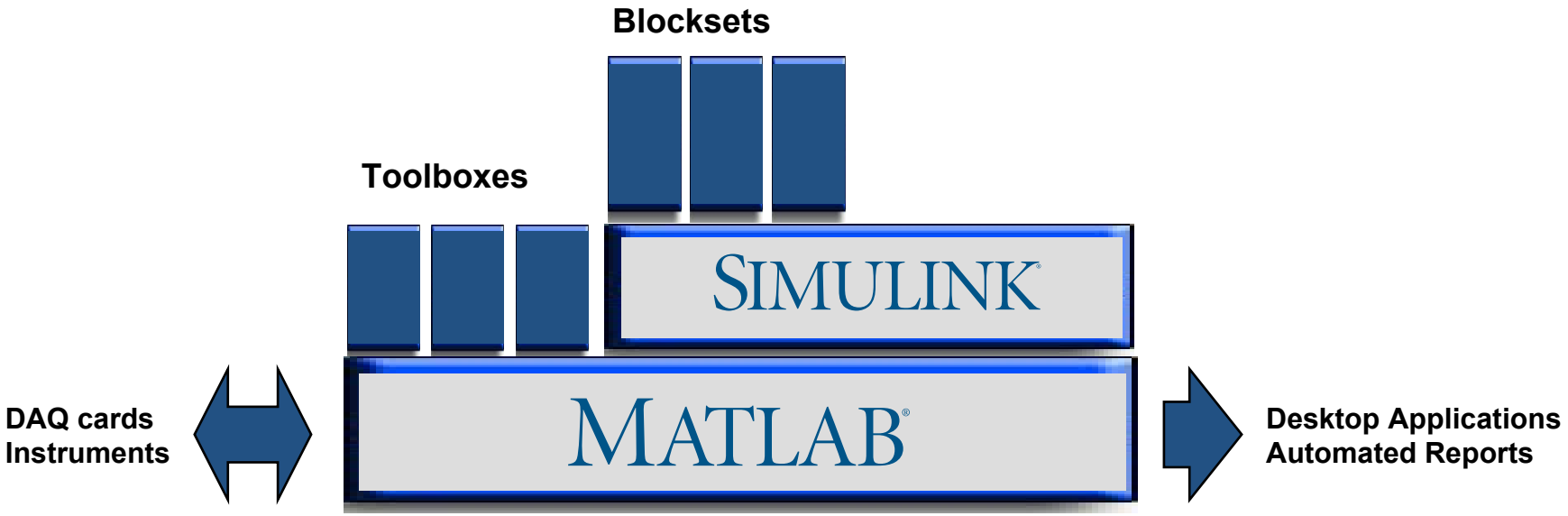
Simulink

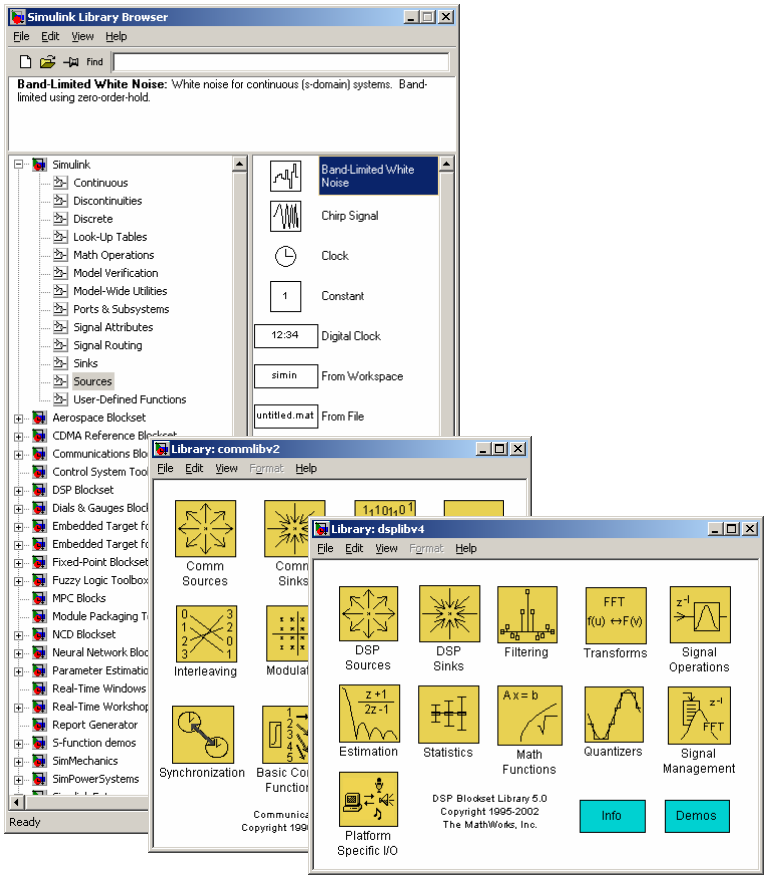


- Hierarchical block diagram design and simulation tool
- Digital, analog/mixed signal and event driven
- Visualize Signals
- Co-develop with C code
- Integrated with MATLAB

Simulink in The MATLAB Environment



The Simulink Block Libraries

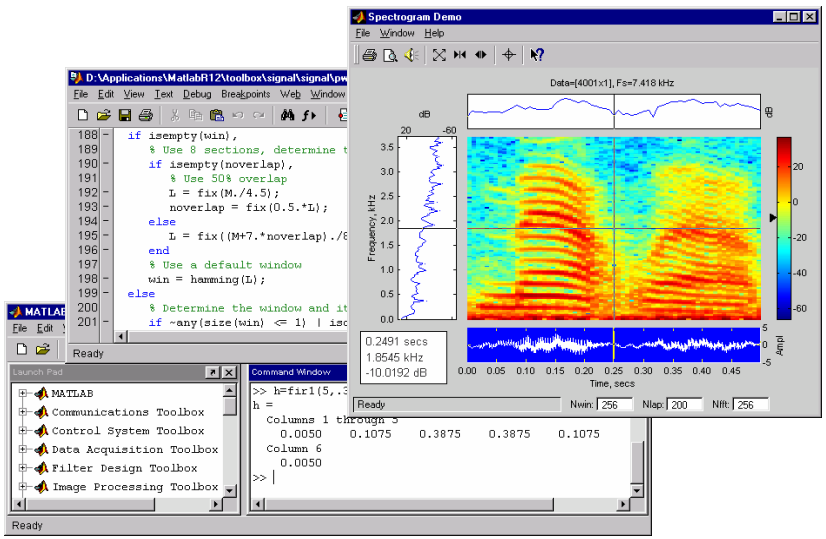


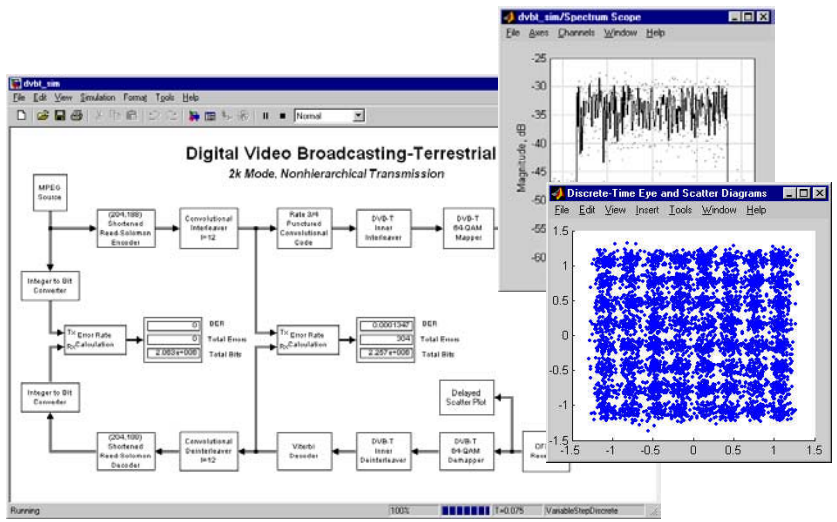
- Simulink
  - Sources and sinks
  - Continuous and Discrete
  - Math, Non-Linear
  - Look-up tables, user functions
  - Subsystems, verification
- DSP Blockset
  - Sub libraries
- Communications Blockset
  - Sub libraries
- Fixed-Point Blockset
- Power-Systems Blockset
- Incremental development

S/W Demonstration: Build

The MathWorks products for DSP and Communications

- Accelerating engineering design and discovery
- MATLAB for algorithm development and analysis
- Simulink for system-level design





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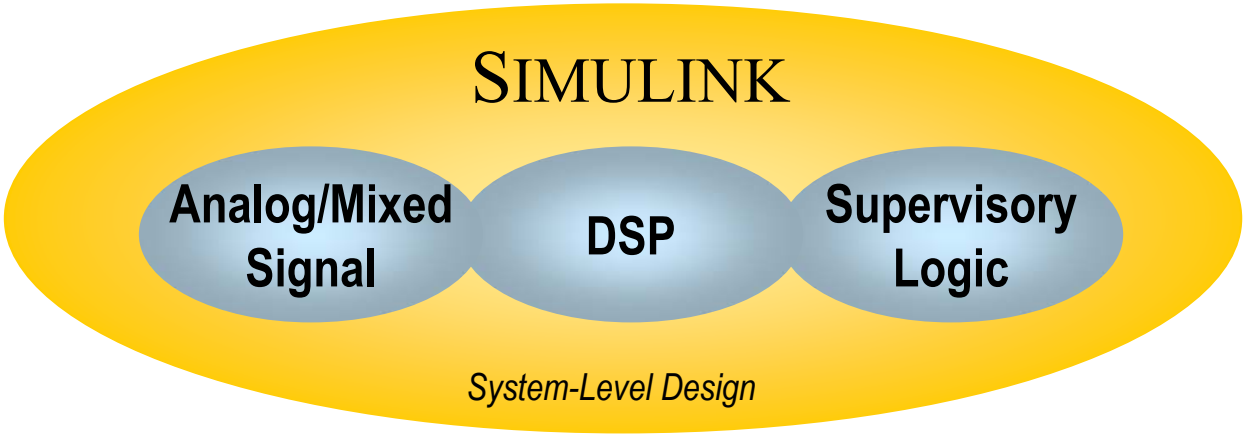
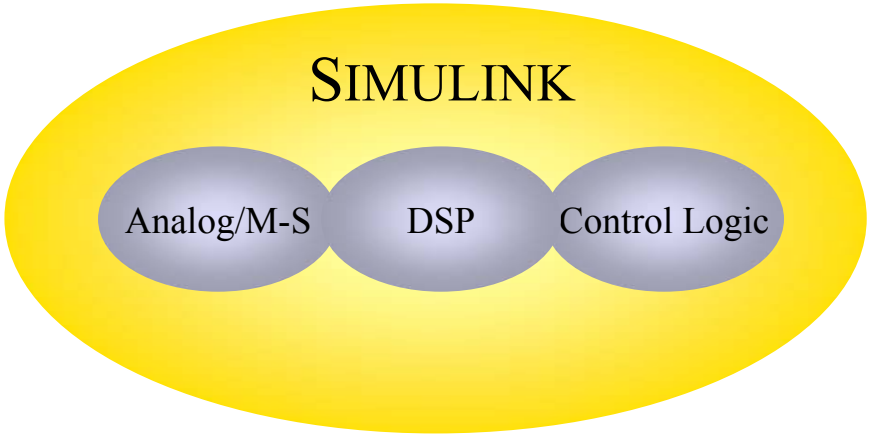
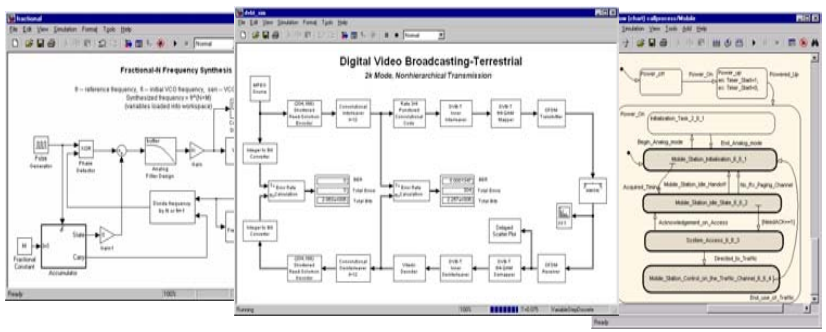


Common tool for all design teams
Simulate component interactions
Test behavior of whole system
No re-design necessary

Modeling system components

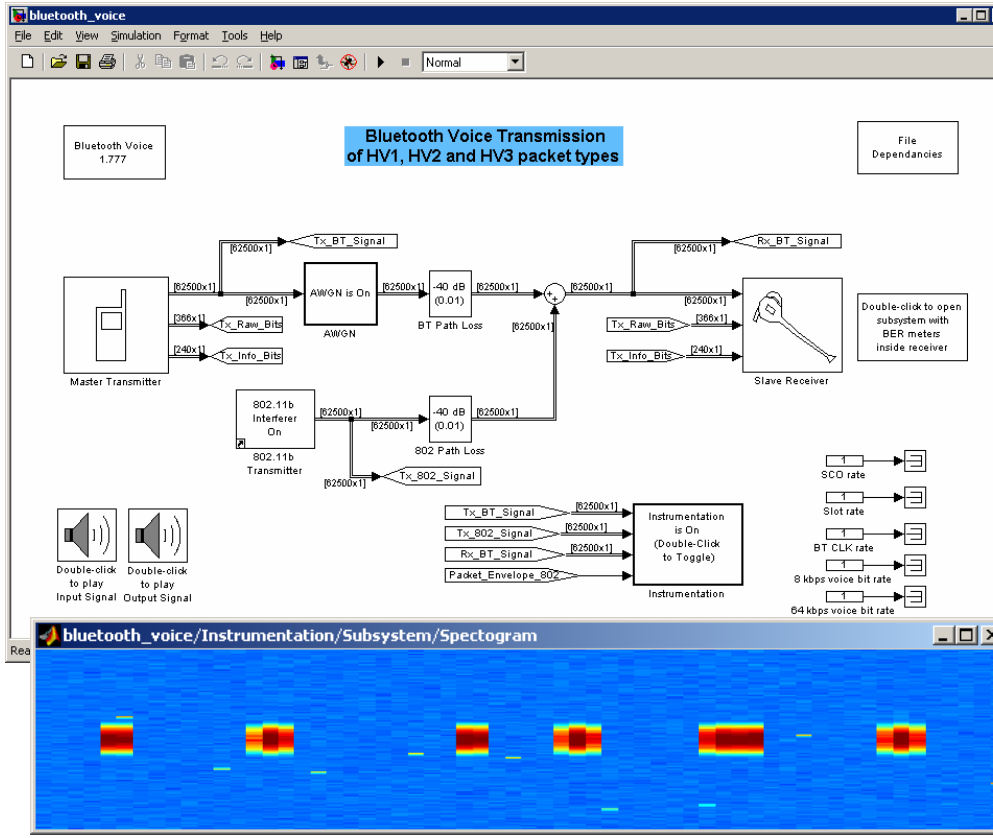




- Analog/Mixed-Signal
  - E.g. PLLs, data converters
  - Continuous time, variable-step ODE solvers
- DSP
  - E.g. Baseband processing, speech processing
  - Discrete time, fast frame-based processing. Bit-true cycle accurate.
- Control Logic
  - E.g. MAC layer, acknowledgement schemes
  - Reactive or event driven state machines

End-to-end systems

- Digital and analog operations such as coding, interleaving and modulation
- Channel models, error coding, sources, sinks
- Multiple rates for frames, symbols, bit and sample rates
- Synchronization
- Performance testing
- Analog, digital, hybrid, and event-driven simulation



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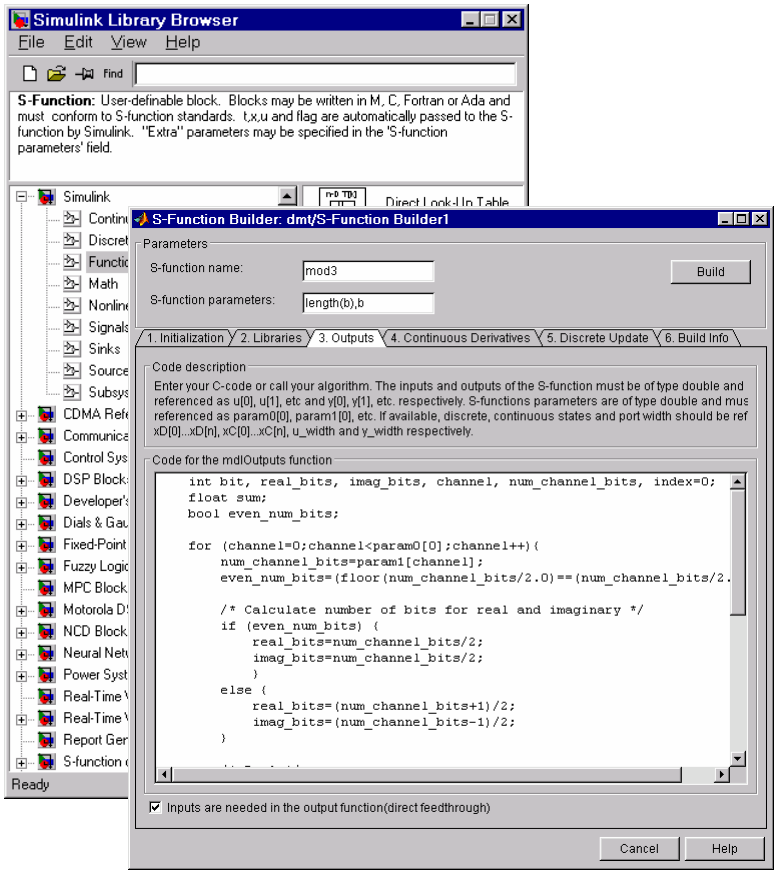
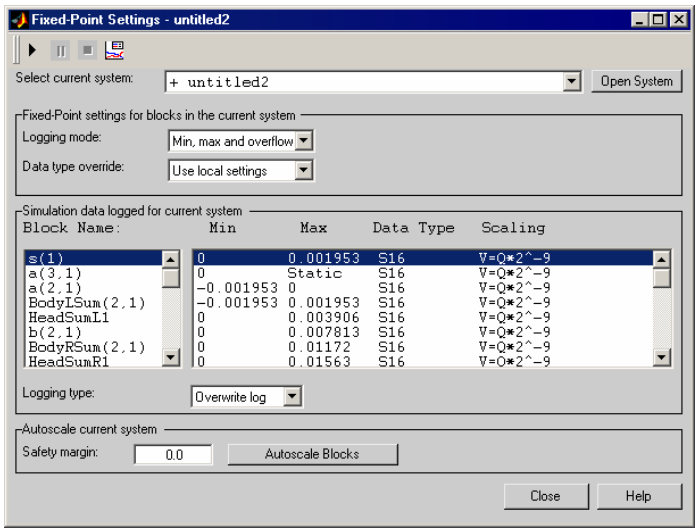
Co-develop with C Code

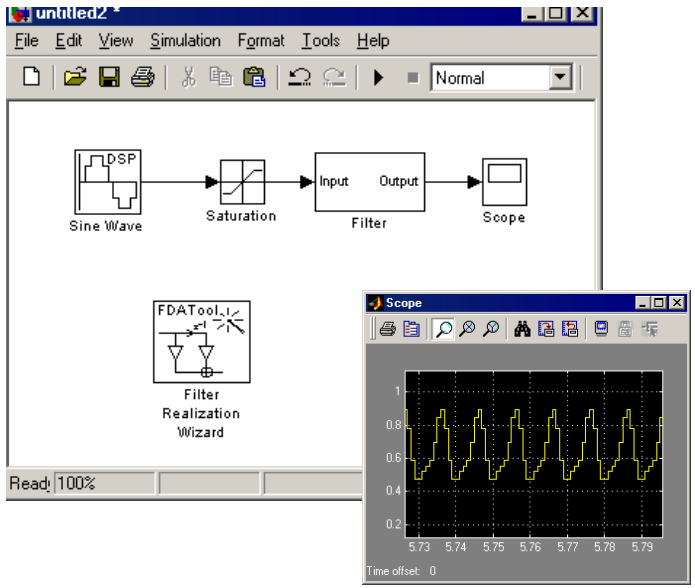


- S-function block in Simulink
  - API to specify outputs, state, parameters and sample-times
- S-function builder in Simulink
  - GUI to enter C Code
  - Predefined variables for input, output and states

Fixed Point Simulation

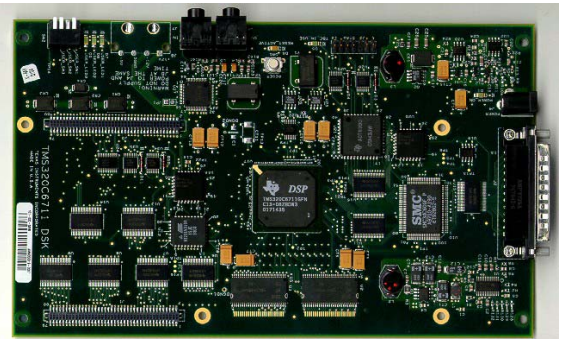
- New integrated fixed point in core Simulink (R13)
- User-definable data types
- Analysis tools
  - log min, max, overflows block-by-block
- Floating point override options





Links to implementation

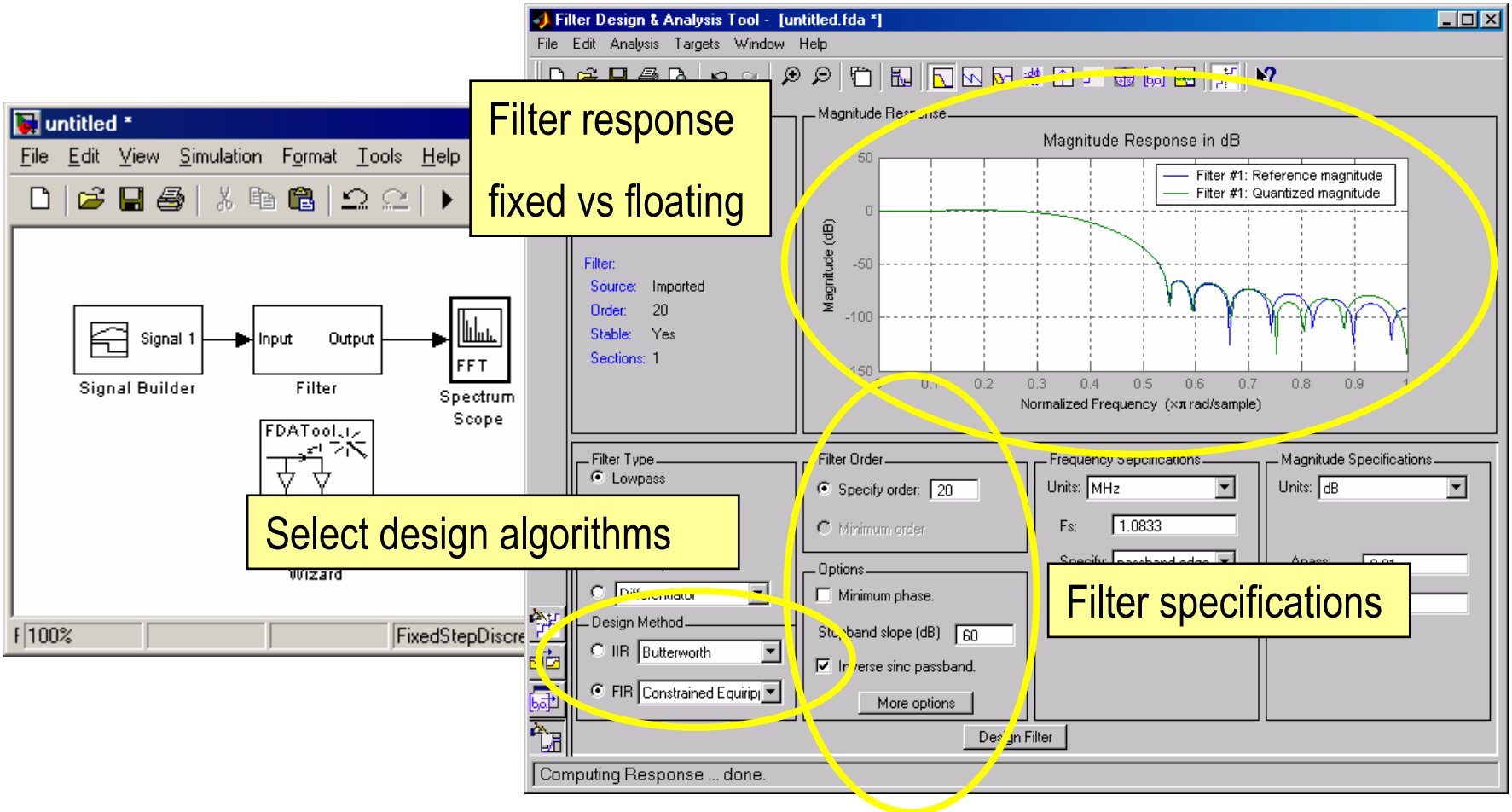
- Real-Time Workshop
  - Automatically generates ANSI C from Simulink
  - Customizable code
  - Rapid Prototyping



- Embedded Targets
  - TI C6000
  - Motorola MPC555

- Altera DSP Builder
  - Bit-true and cycle-true Simulink library for common functions
  - Automatic HDL code generation from a Simulink model
  - Available from Altera

FIR Filter Design: demo



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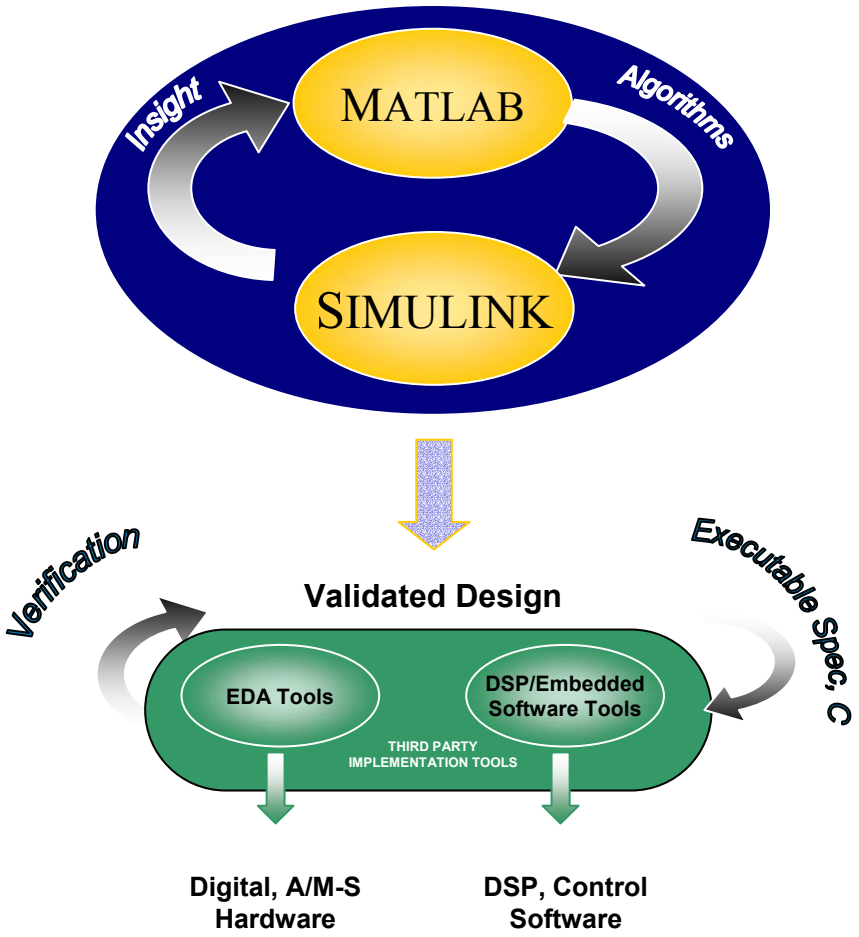
Summary

ALTERA.

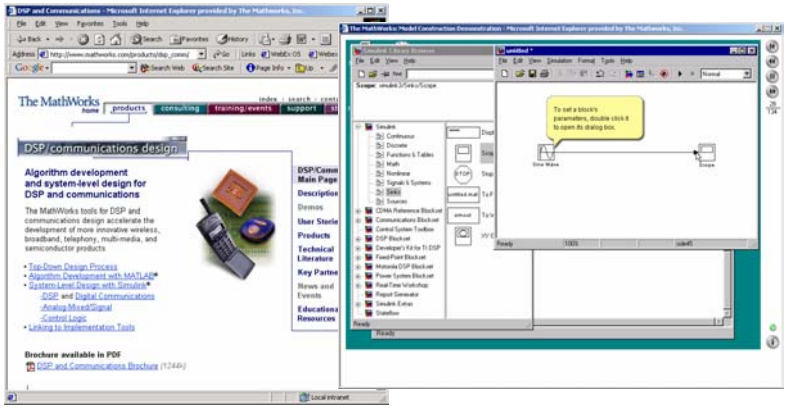
MATLAB and Simulink



- Create validated design
- Use as reference or executable specification to test low-level designs against
- Provide clear specifications
- Detect design flaws early
- Reduce risk and time-to-market

Further Information on Products and Services

- Product information and animated demonstrations
  - www.mathworks.com/products/dsp_comm
- Events
  - www.mathworks.com/dsp_events
  - Regular on-line software demonstrations



MATLAB Central

- www.mathworks.com/matlabcentral
- MathWorks and user contributed models