



SOPC
WORLD
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MathWorks Integrated Design Solution

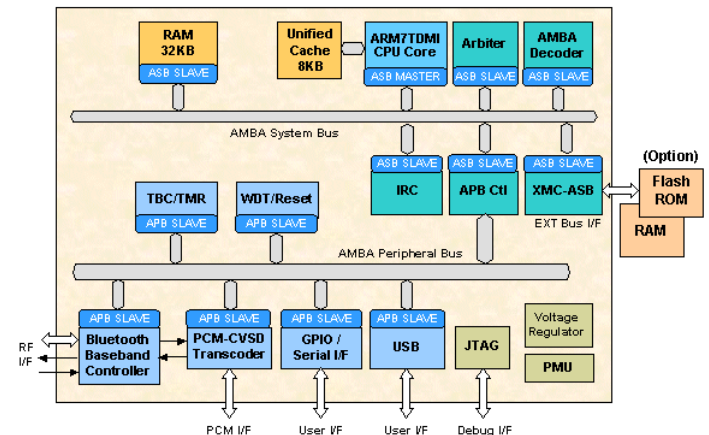
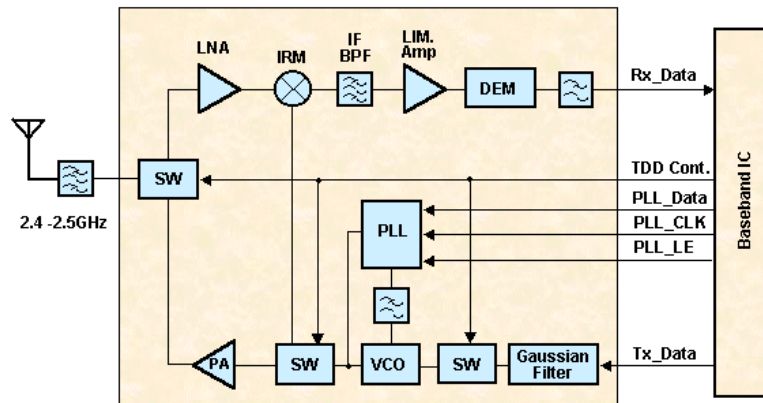
The MathWorks at a Glance

- Founded in 1984, privately held
- Headquarters in Natick, Massachusetts (near Boston)
- European offices in the UK, France, Germany, Switzerland, Italy, Spain, and Benelux region
- Over 1000 employees, including $\frac{1}{3}$ in product development
- More than 500,000 users in 100 countries, on all seven continents!



Today's System and IC Design Challenges

- Hardware: RF/Analog, Digital IC, FPGA
- Software: DSP, MAC, Control, Use interface
- Moving partitioning boundaries
 - Analog ↔ Digital IC ↔ FPGA ↔ DSP S/W ↔ Micro controller S/W
- Implementation specific tools lock your IP into one target type
 - Spice, HDL, ASM , C/C++

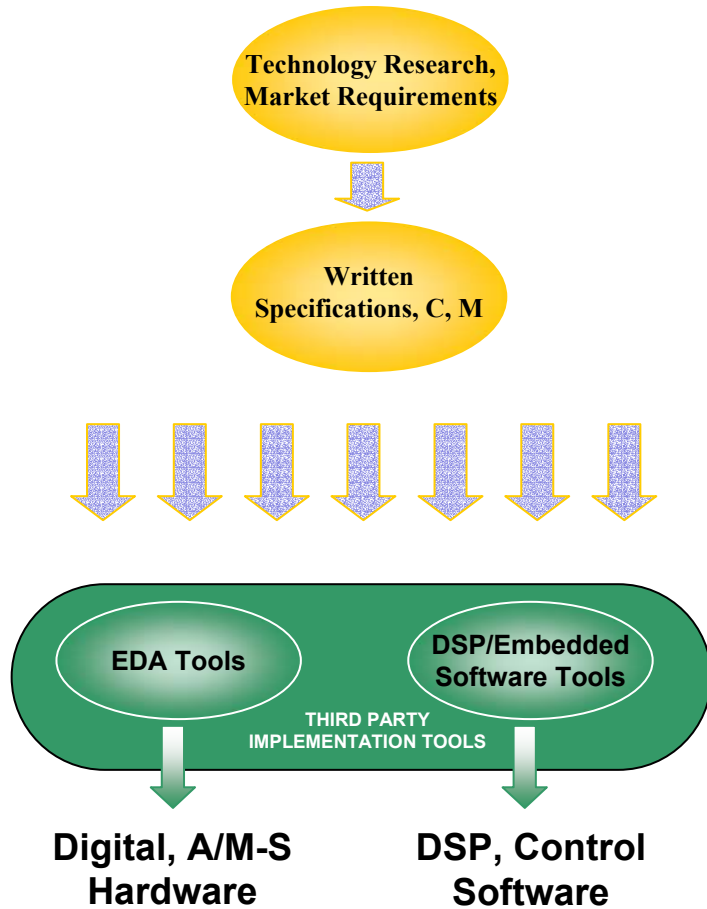


Today's Business and Organization Challenges

- Time-to-market pressure
 - A few months delay has huge revenue impact
- Team integration
 - Analog/Mixed-Signal, Digital hardware, DSP S/W, Control S/W teams
 - All speak a different language and communicate via written documents
- Increasing ASIC mask costs



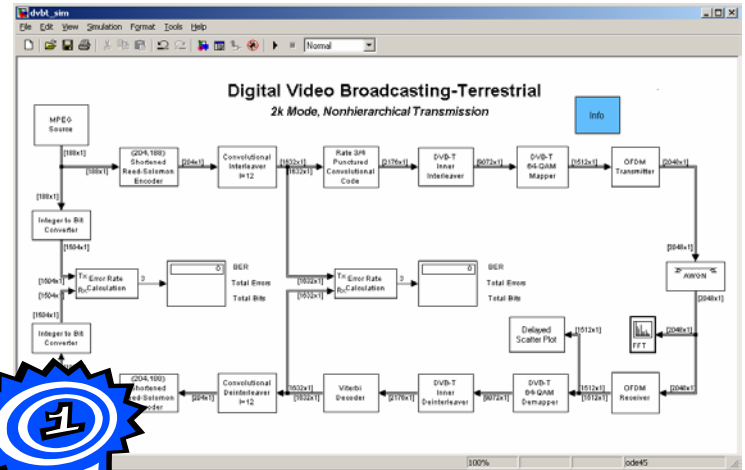
Traditional Flow: Little or No Early Simulation



- Technology research and market requirements
- Systems engineering
- Partition into components create written specifications for teams
- Minimal or no simulation. C, M
- Design failure risk high. Flaws detected late, during circuit level, RTL or C/ASM code design
- Risk of time-to-market delays

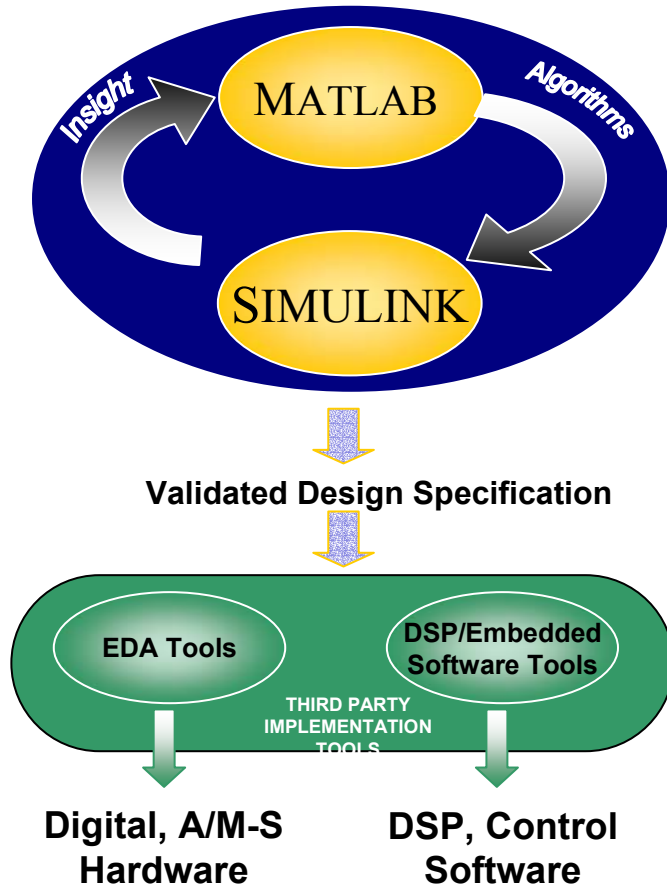
What if You Could...?

- Build a model of a complete system in minutes or days
- Simulate the behavior of the whole system before starting low-level design work?
 - Analog, digital and control together
 - Test for design flaws early
 - Trade-off architectures and parameter in minutes find best design
- Communicate your ideas and share with other teams?
- Keep your IP in an implementation neutral tool as long as possible?
- Only start development with a validated, fully tested design?



The MathWorks System-Level Solution

- MATLAB and Simulink
- Before circuit level, RTL or C/ASM code design
- Create a validated reference design

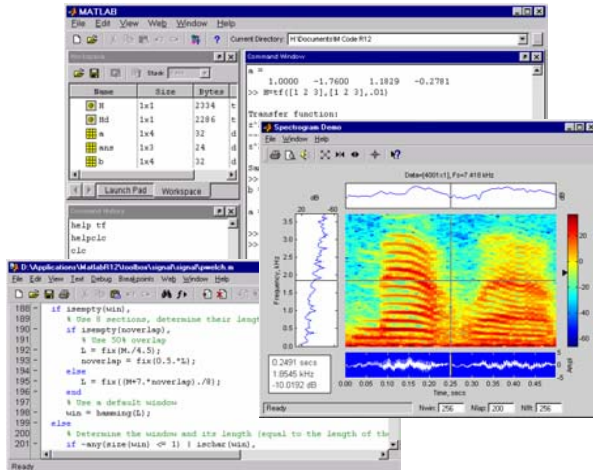


```
1.0000 -1.7600 1.1829 -0.2781
>> hztf([1 2 3],[1 2 3],.01)
Transfer function:
s^2 + 2 z + 3
-----
s^2 + 2 s + 3
Sampling time: 0.01
>> [b,a] = butter(3,.2)
b =
0.0181 0.0543 0.0543 0.0181
a =
1.0000 -1.7600 1.1829 -0.2781
>> hztf(b,a,.01)
Transfer function:
0.0181 s^3 + 0.0543 s^2 + 0.0543 s + 0.0181
-----
s^3 - 1.76 s^2 + 1.183 s - 0.2781
Sampling time: 0.01
>> |
```

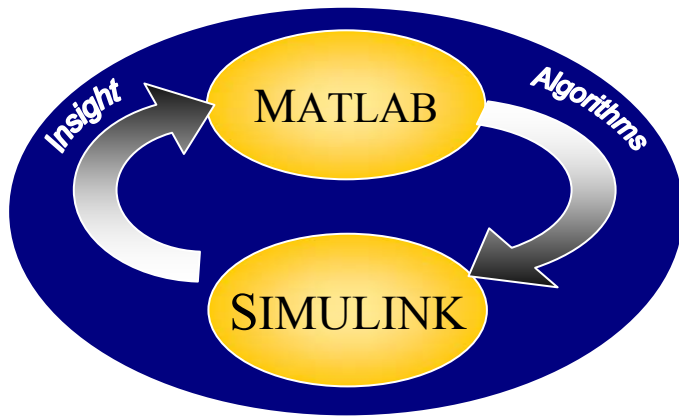
MATLAB

MATLAB

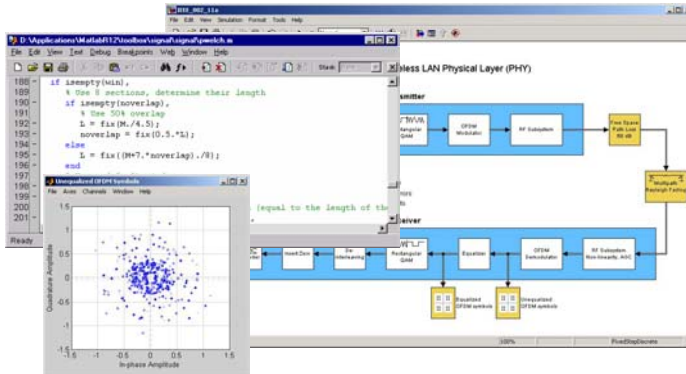
- Research new technology
- Perform mathematical modeling
- Development algorithms
- Acquire, visualize and analyze data



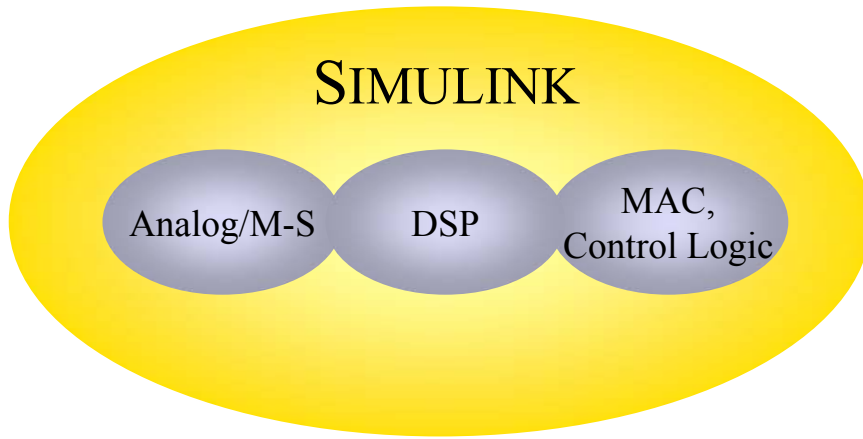
Simulink



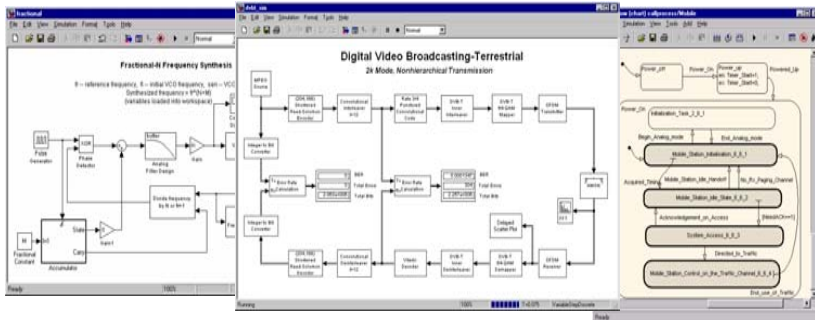
- Graphically design architecture and simulate behavior of whole system. Bit-true cycle accurate.
- From libraries of pre-built blocks
- Import C or MATLAB Code
- Test, optimize, explore parameter and architecture trade-offs



Model Different Components

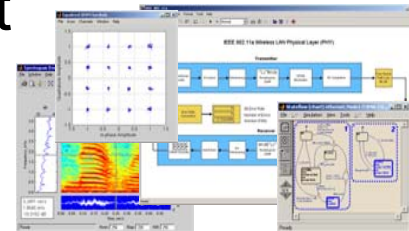
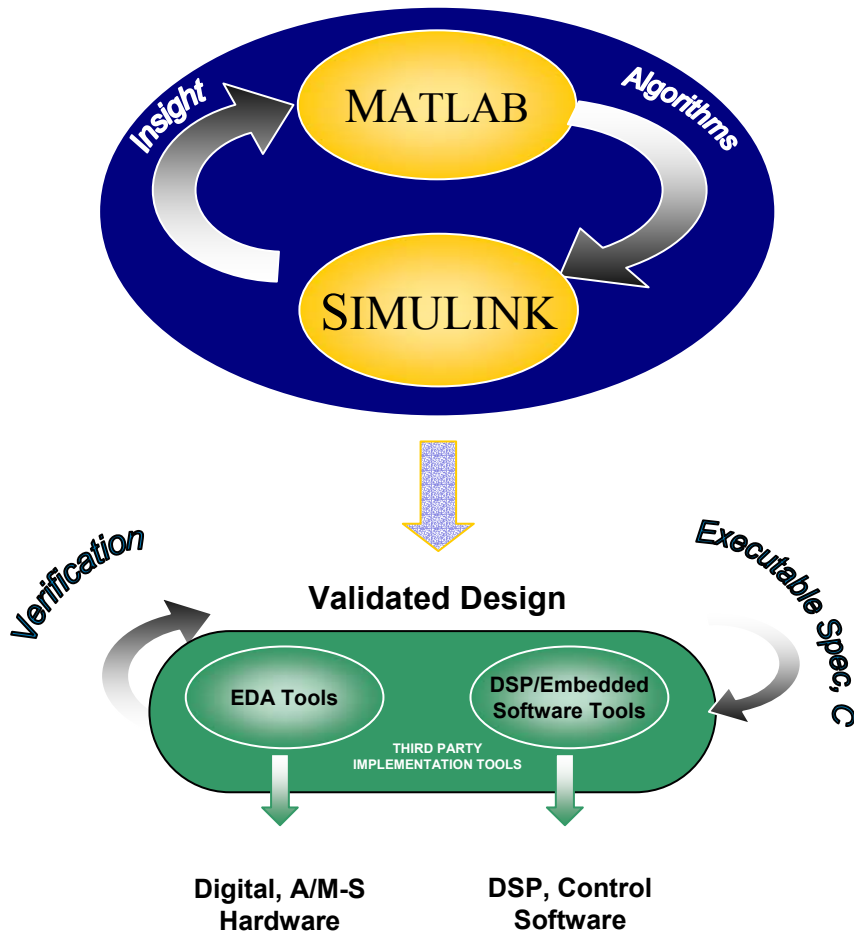


- Analog/Mixed-Signal
 - PLLs, data converters
 - Continuous time, variable-step ODE solvers
- DSP Baseband
 - Discrete time, fast frame-based processing. Bit-true cycle accurate.
- MAC layer/Data Link Layer
 - Simple protocols, acknowledgement schemes
 - Reactive or event driven state machines
 - With Stateflow



Use a Validated Design

- Create **validated design**
- Use as reference or executable specification to test low-level designs against
- Provide clear specifications
- Detect design flaws early
- Reduce design risk and time-to-market



Motorola's Wireless Subscriber Systems Group

■ Challenge

- Mixed-signal Phase-Locked Loop (PLL) design
- Cycle-to-cycle jitter and loop locking sensitivity
- SPICE/Verilog
- 100 μ secs: 2 hours

■ Solution

- Simulink
- Faster development time and simulation time
- 100 μ secs : 2.5 mins
- Sub-picosecond resolution

“ *The Simulink models exceeded our project specifications for required simulation speed. Accurate simulations can now be measured in minutes rather than hours or days.* ”

Yuan Yuan, Motorola

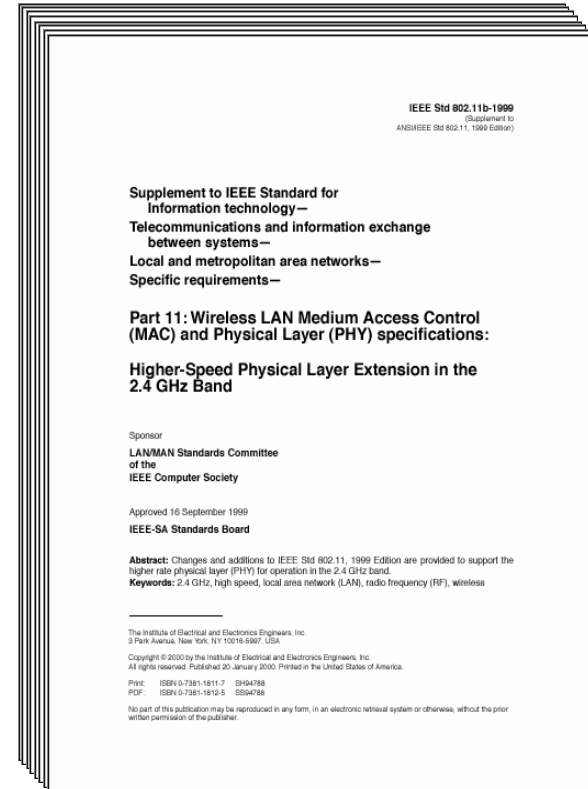
PHY Design Case Study: IEEE 802.11b

■ IEEE Standard Document

- 600 pages (11 + b appendix)
- 4 modes (1, 2, 5.5 and 11Mbps)

■ Components

- Framing and CRC
- Long/short preamble and sync
- Modulation and spreading
- Filtering
- Channel number selection (1-11)
- RF subsystems, Tx power, mask, power-on ramp



1Mbps Mode

- Modulation
 - DBPSK
- Spread
 - 11 chips Barker sequence per symbol
- Pulse shaping
 - 4/8 samples per chip
 - Root raised cosine
- Channel
 - AWGN

The leftmost chip shall be output first in time. The first chip shall be aligned at the start of a transmitted symbol. The symbol duration shall be exactly 11 chips long.

15.4.6.4 Modulation and channel data rates

Two modulation formats and data rates are specified for the DSSS PHY: a *basic access rate* and an *enhanced access rate*. The basic access rate shall be based on 1 Mbit/s DBPSK modulation. The DBPSK encoder is specified in Table 65. The enhanced access rate shall be based on 2 Mbit/s DQPSK. The DQPSK encoder is specified in Table 66. (In the tables, π shall be defined as counterclockwise rotation.)

Table 65—1 Mbit/s DBPSK encoding table

Bit input	Phase change (π)
0	0
1	π

Table 66—2 Mbit/s DQPSK encoding table

Dibit pattern (d0,d1) d0 is first in time	Phase change (π)
00	0
01	$\pi/2$



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C/C++

```
Microsoft Visual C++ [D:\... \bin\source\main.cpp]
File Edit View Insert Project Build Tools Window Help
[D:\...] \bin\source\main.cpp
[Global] All global members main
Workspace browser
Source
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```

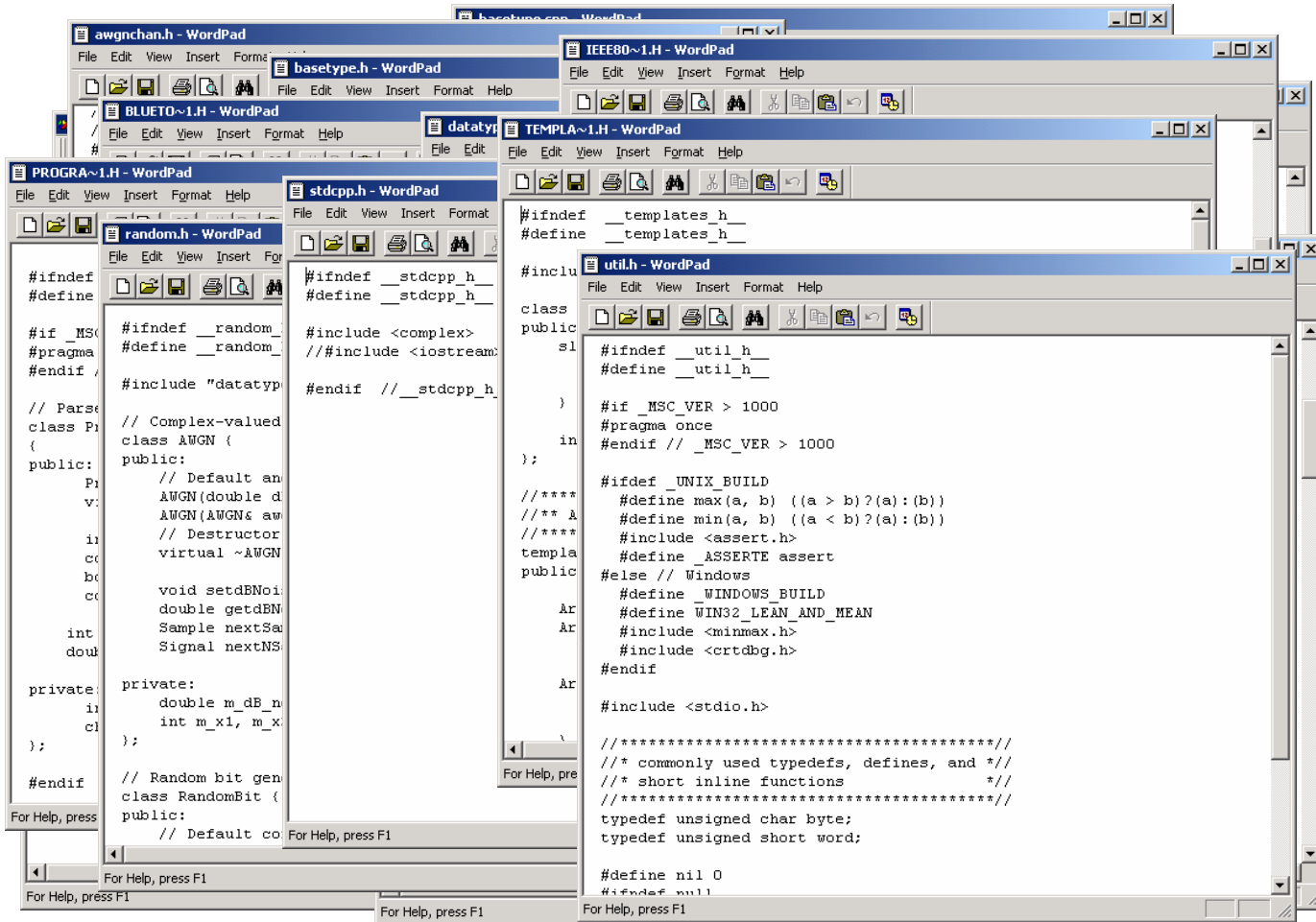


NIST 802.11b and Bluetooth C/C++ Code



- w3.antd.nist.gov/wctg/bluetooth/btint.html
- Bluetooth and 802.11b
- 802.11b
 - Random bits
 - 1 or 11Mbps modulation and spreading
 - Filtering
- Bluetooth
 - Random bits
 - Modulation
 - Filtering

C/C++ Code: 17 Files, 1500-2000 lines



The image shows a collection of overlapping WordPad windows, each displaying a different C/C++ header file. The windows are titled with file names such as 'awgnchan.h', 'basetype.h', 'IEEE80~1.H', 'BLUETO~1.H', 'datatyp', 'PROGRA~1.H', 'stdcpp.h', 'random.h', 'TEMPLA~1.H', and 'util.h'. The code visible in the windows includes preprocessor directives like #ifndef, #define, #include, and #pragma, as well as C++ class declarations and function definitions. For example, the 'random.h' window shows a class 'AWGN' with methods for signal generation and noise addition. The 'util.h' window shows various utility macros and typedefs.



C/C++ Code: Build, Run, Debug, and Change

- Build and run
 - Bug: File I/O
- Speed
 - 7 secs for 100 packets
- Time to create
 - 400 days @ 5 lines/day
 - 40 days @ 50 lines/day
- Removing Bluetooth
 - Difficult. Many implicit dependencies

The screenshot shows the Microsoft Visual C++ IDE. The top window displays the source code for `IEEE802.11b.h`, which includes a copyright notice for the National Institute of Standards and Technology and author information for Amir Soltanian. The bottom window shows the output of the `btint` program, which reports the following details:

```
Deleting intermediate files and output files for project 'btint - Win32 Release'.
Configuration: btint - Win32 Release
Compiling
awgnchan.cpp
basetype.cpp
bluetooth.cpp
ieee802.11b.cpp
main.cpp
programargs.cpp
random.cpp
Linking
Creating browse info fi
btint.exe - 0 error(s).
```

The output window also shows the following parameters:

```
Desired signal transmitter/receiver: BT.
Interference transmitter: 802.11.
Number of packets = 1.
Packet length = 160.
Frequency offset (MHz) = 4
Carrier-to-interference ratio (dB) = 100.
Carrier-to-noise ratio (dB) = 360.
Number of bit errors = 0.
BER = 0.00e+000.
Press any key to continue_
```

D:\>btint -c 100 -d 802.11 -i BT -EbNo 6

S/W Demonstration

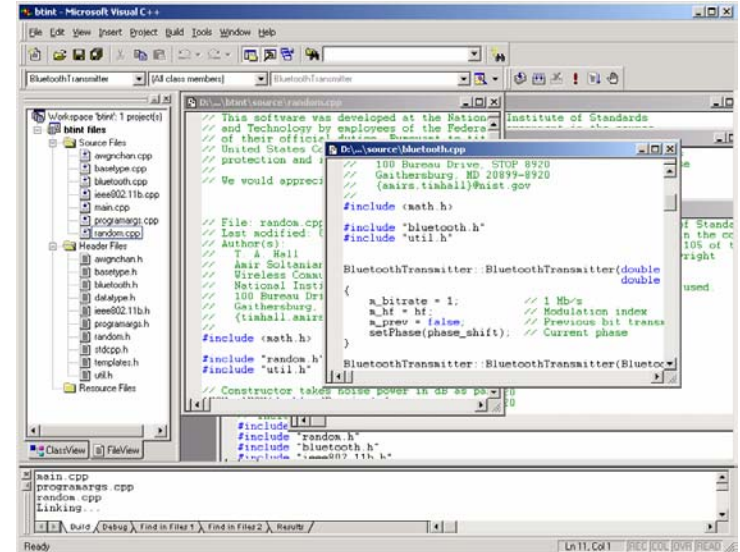
C/C++ Pros and Cons

■ Pros

- Ubiquitous
- Fast to execute
- Data type options

■ Cons

- No canned DSP/Comm functions
- Can't visualize signals
- Too low-level, lots housekeeping
- Error prone design entry, implicit interdependencies
- Slow to iterate, debug and make changes

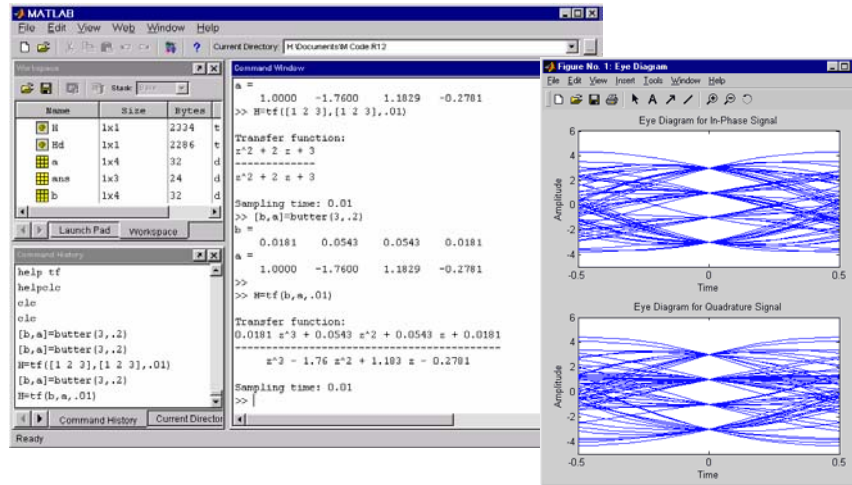




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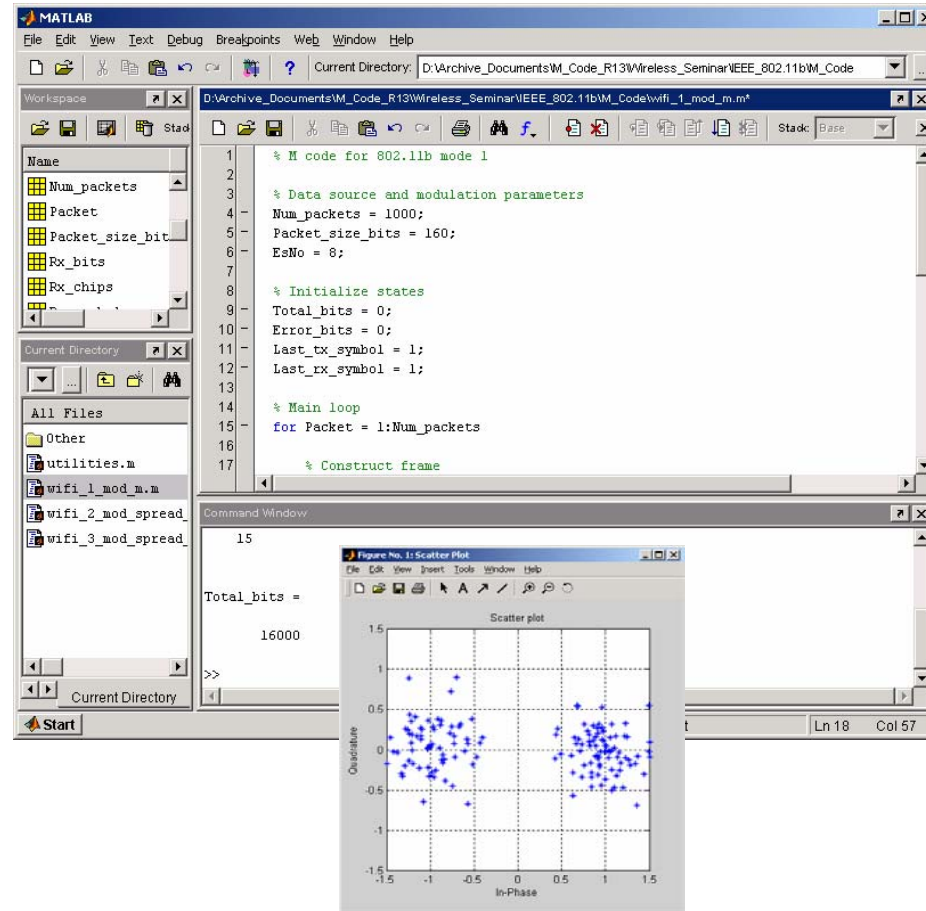


MATLAB



802.11b: M Code

- Using MATLAB
 - Generating bits
 - Symbols and noise
 - `scatterplot(Rx_symbols)`
- 802.11 Tx lines of code
 - One single file 52 lines
 - Modulation (3 lines)
 - Spreading (1 line)
- Speed
 - 2 secs for 100 packets
- Find the bug



S/W Demonstration: Build and show

MATLAB Vs C/C++: Spreading and Upsampling

■ C Code

```
Bits spread=addChips(diffOut[slice(i,1)]);
```

Bits

```
IEEE802_11b_Transmitter::addChips(const Bits& input) {  
    Bits spreadOut(input.size()*Ns,false);  
    for (int i=0;i<input.size();++i){  
        for(int j=0; j<11; ++j) {  
            spreadOut[i*Ns+4*j]= m_chip[j]^input[i];  
        }  
    }  
    return spreadOut;  
}
```

■ M Code

```
Tx_chips=reshape(Barker*Tx_symbols',[ ],1);  
Tx_samples(1:Samples_per_chip:end)=Tx_chips;
```

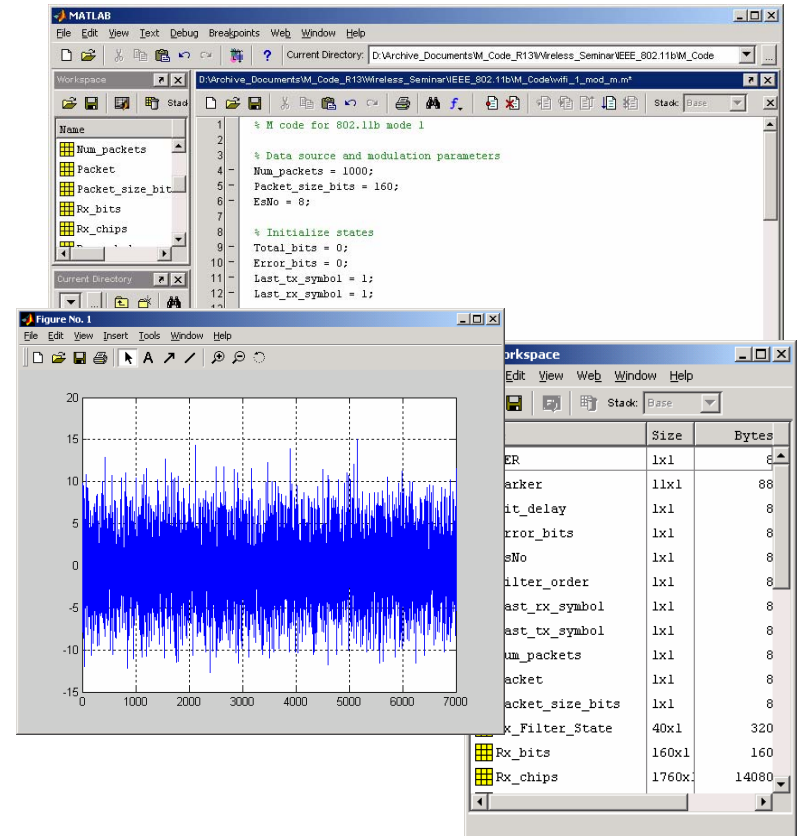
MATLAB Pros and Cons

■ Pros

- Interactive
- Easy signal visualization
- Canned common functions
- Faster development

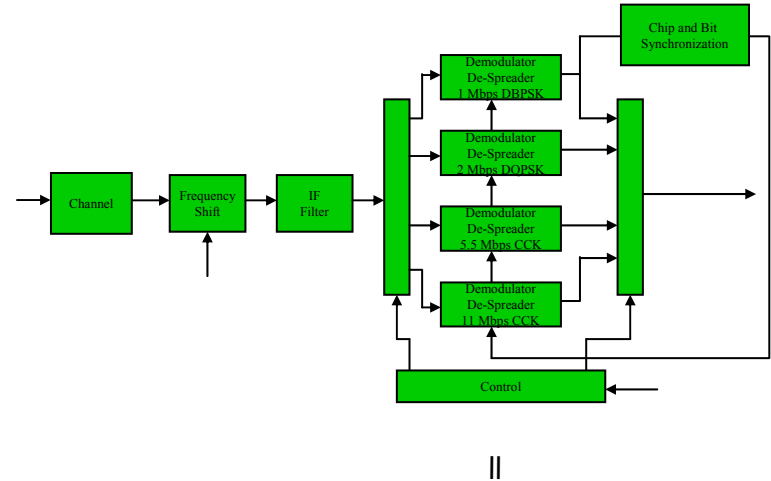
■ Cons

- Limited data types
- Limited low-level control
- Less memory efficient
- Slower to execute for scalars, loops before R13



Limitations of C and M for System Design

- No architecture information
 - Can only model a pipeline
 - Can't describe a real system
- No timing information
 - Can only model uniform Fs
 - Difficult to model delays
 - Must manually handle state
 - Can't model A/M-S
 - Difficult to model Rx algorithms



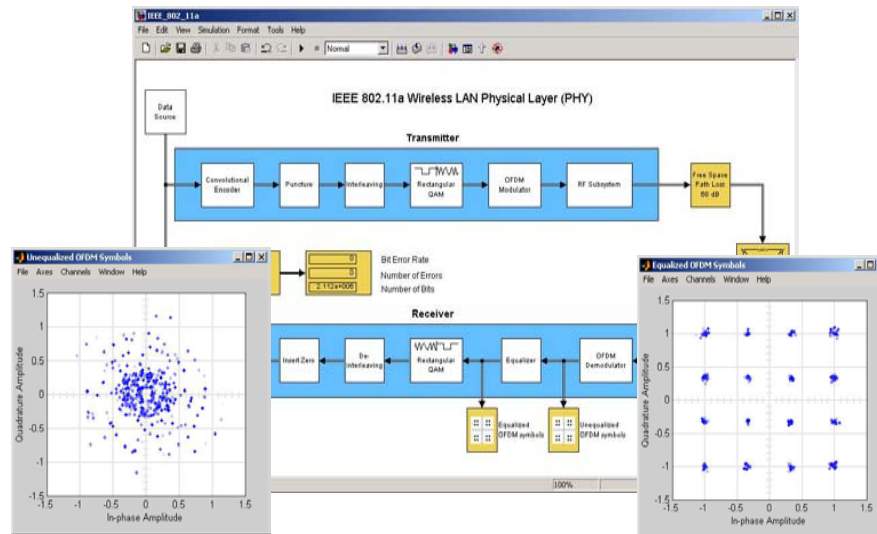
```
1 % M code for 802.11b mode 1
2
3 title
4 % Data source, channel and modulation parameters
5 Num_packets=100;
6 Packet_size_bits=100;
7 E2B0=0;
8
9 % Spreading parameters
10 Backer=[1 -1 1 -1 1 -1 1 -1 -1 -1];
11 Spreading_rate=length(Backer);
12
13 % Filter parameters
14 Samples_per_chip=4; % Samples_per_chip to make delay calc easy
15 Bit_delay=1;
16 Filter_order=40; % Multiple of 4
17
18 % Filter state
19 Tx_filter_state=ones(1,Filter_order); % Full filter with w = +1 symbol
20 Rx_filter_state=ones(1,Filter_order); % Full filter with w = +1 symbol
21
22 % Initialization
23 Tx_bits_delayed_state=0;
24 Rx_bits_delayed_state=ones(1,Filter_order); % Full filter with w = +1 symbol
25
26 % Initialization
27 Tx_bits=0;
```




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Simulink



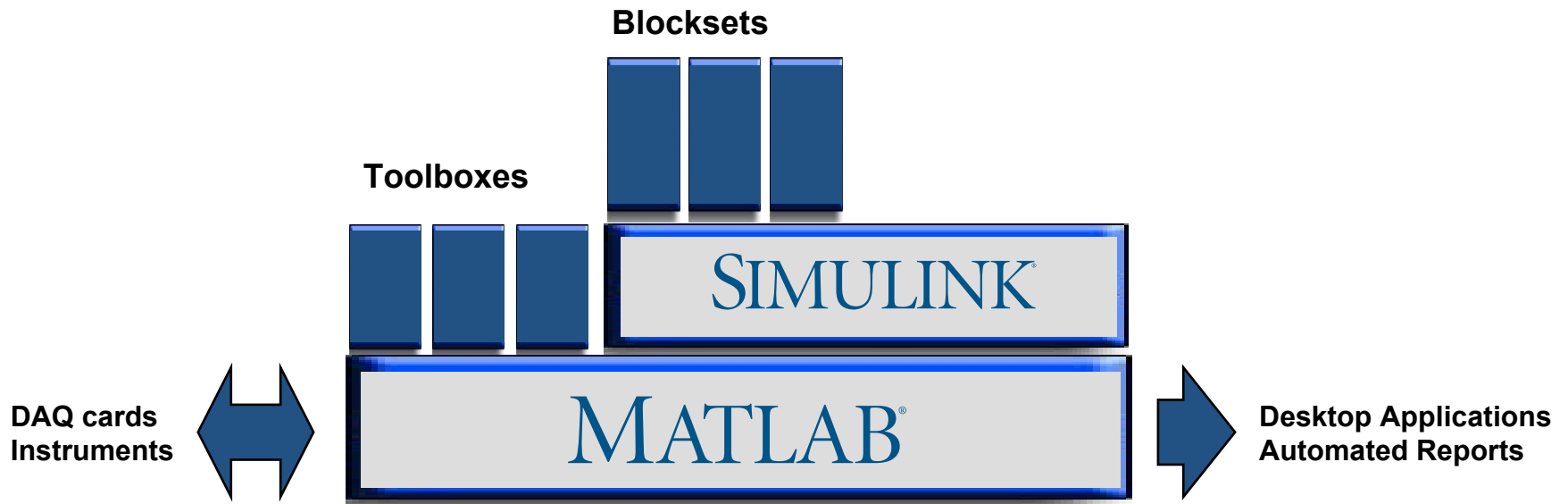
Simulink

The screenshot displays the Simulink environment with several windows open:

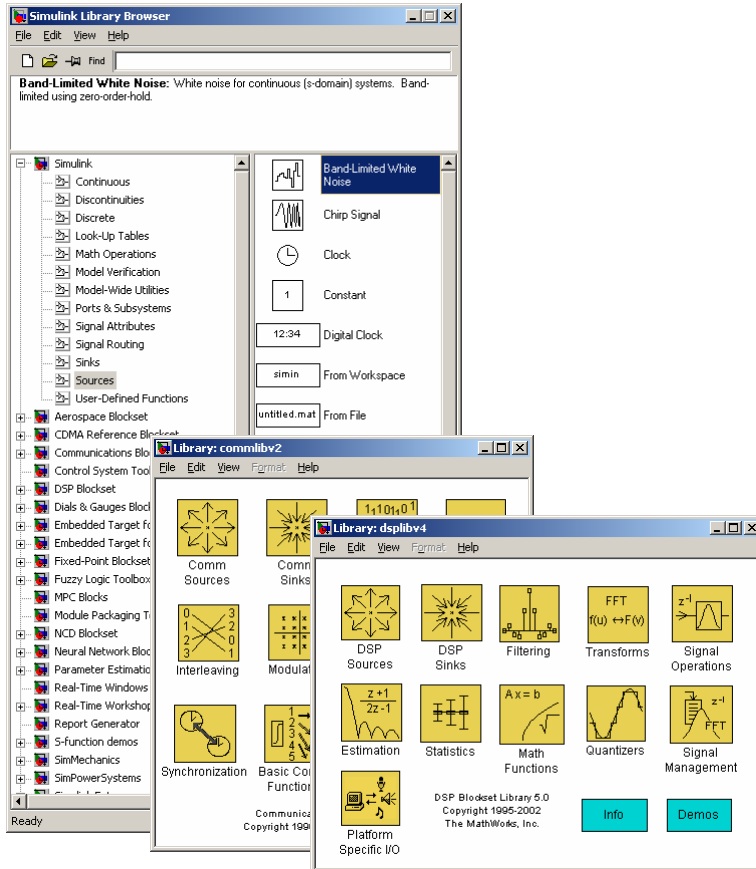
- Model Browser:** Shows a hierarchical tree of blocks including 'Base Station', 'Calculate Tx Power', 'Channel', 'Mobile', 'Access Amplify', 'Channel Coding, Interleaving and Modulation', 'IS-95A Rev C Channel', 'Binary to Bit', 'Discrete', 'Downsample', 'Rebuffer', and 'Rebuffer1'.
- Block Diagram:** A central workspace showing a block diagram with inputs like 'Rx_Access' and 'Access_Threshold', and outputs like 'Access_Detect', 'BS_Timed_Out', and 'Power_Bit'. A 'Control Signal' window is overlaid on the diagram, showing a plot of a signal over time.
- MATLAB Code Editor:** Displays C code for a function named 'mdlOutputs'. The code includes comments and a loop for calculating outputs.
- Command Window:** Shows MATLAB commands being executed, such as 'for EbNo = 2:1:6, sim('system'), end'.

- Hierarchical block diagram design and simulation tool
- Digital, analog/mixed signal and event driven
- Visualize Signals
- Co-develop with C code
- Integrated with MATLAB

Simulink in The MATLAB Environment



The Simulink Block Libraries



■ Simulink

- Sources and sinks
- Continuous and Discrete
- Math, Non-Linear
- Look-up tables, user functions
- Subsystems, verification

■ DSP Blockset

- Sub libraries

■ Communications Blockset

- Sub libraries

■ Fixed-Point Blockset

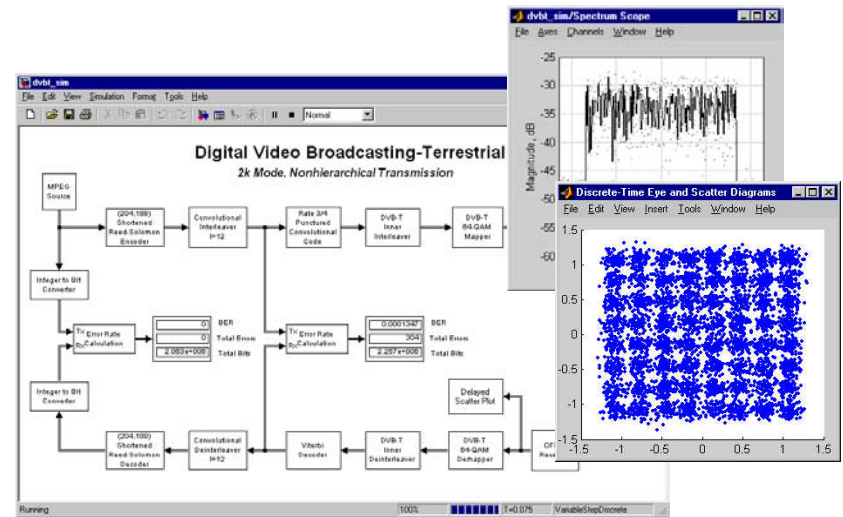
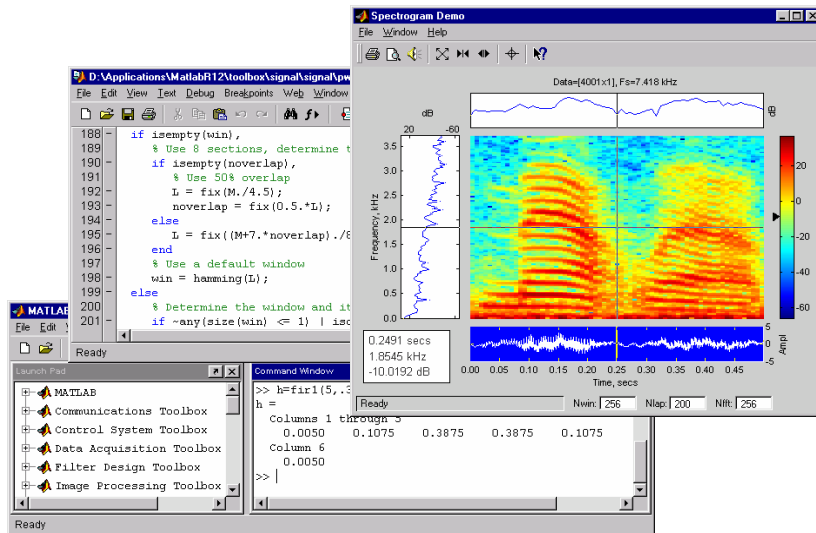
■ Power-Systems Blockset

■ Incremental development

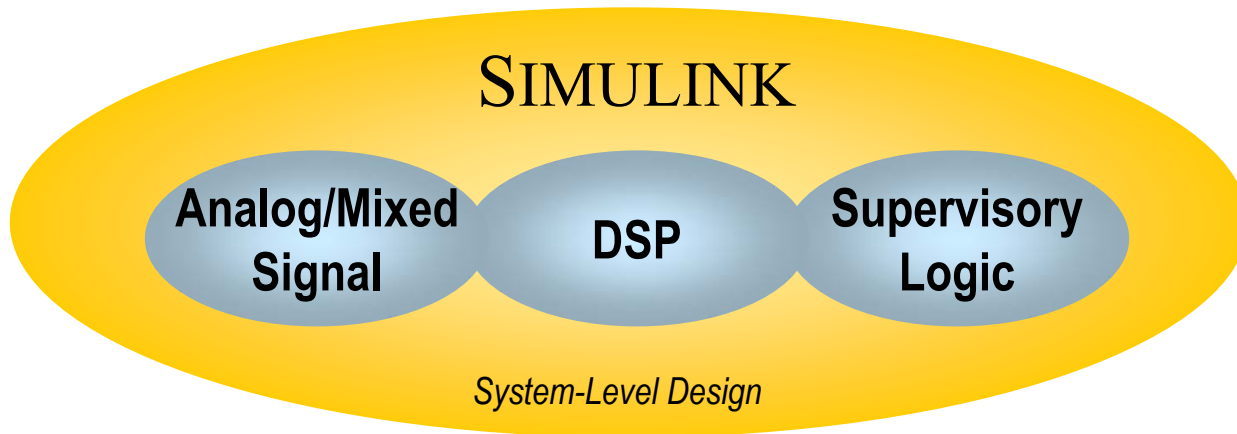
S/W Demonstration: Build

The MathWorks products for DSP and Communications

- Accelerating engineering design and discovery
- MATLAB for algorithm development and analysis
- Simulink for system-level design



MathWorks Integrated Design Solution



Common tool for all design teams
Simulate component interactions
Test behavior of whole system
No re-design necessary

Modeling system components

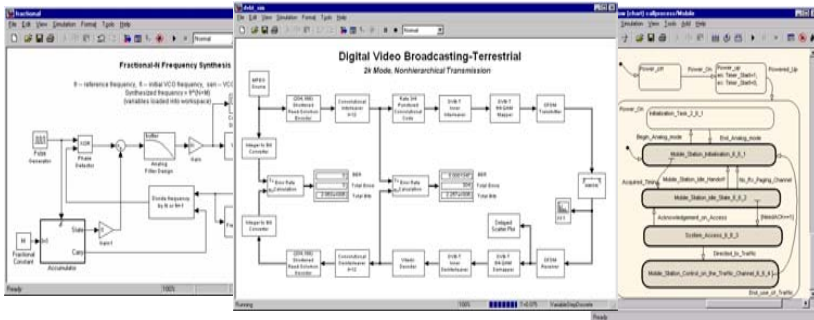
SIMULINK

Analog/M-S

DSP

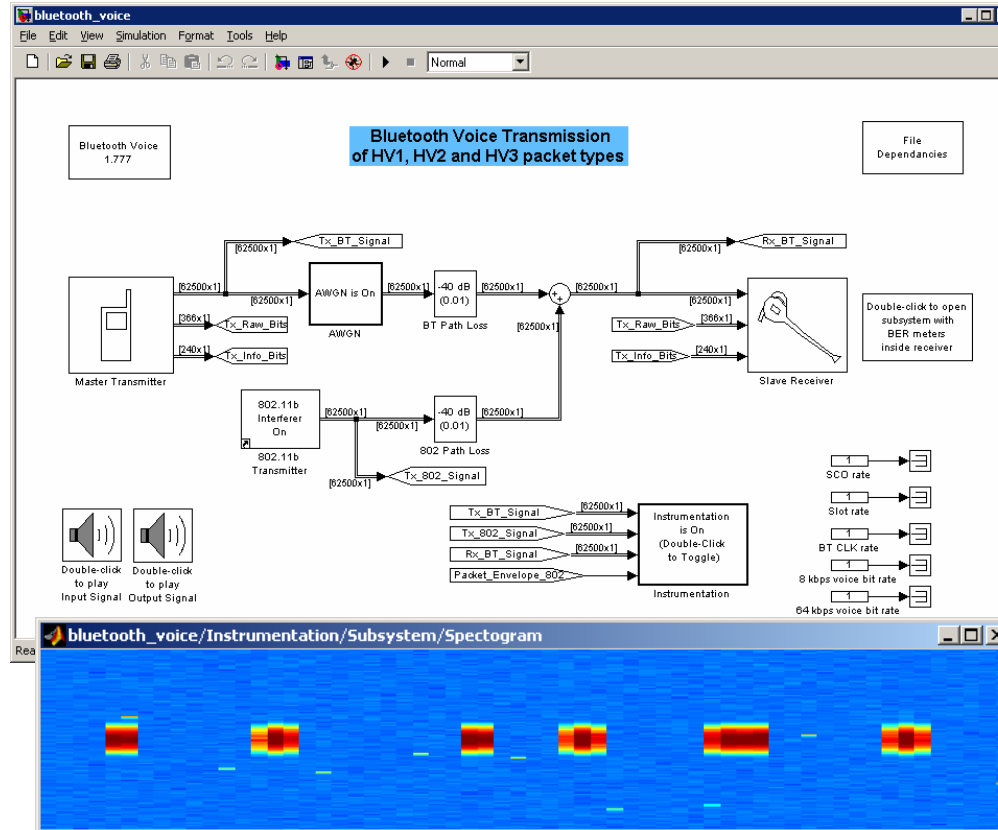
Control Logic

- Analog/Mixed-Signal
 - E.g. PLLs, data converters
 - Continuous time, variable-step ODE solvers
- DSP
 - E.g. Baseband processing, speech processing
 - Discrete time, fast frame-based processing. Bit-true cycle accurate.
- Control Logic
 - E.g. MAC layer, acknowledgement schemes
 - Reactive or event driven state machines



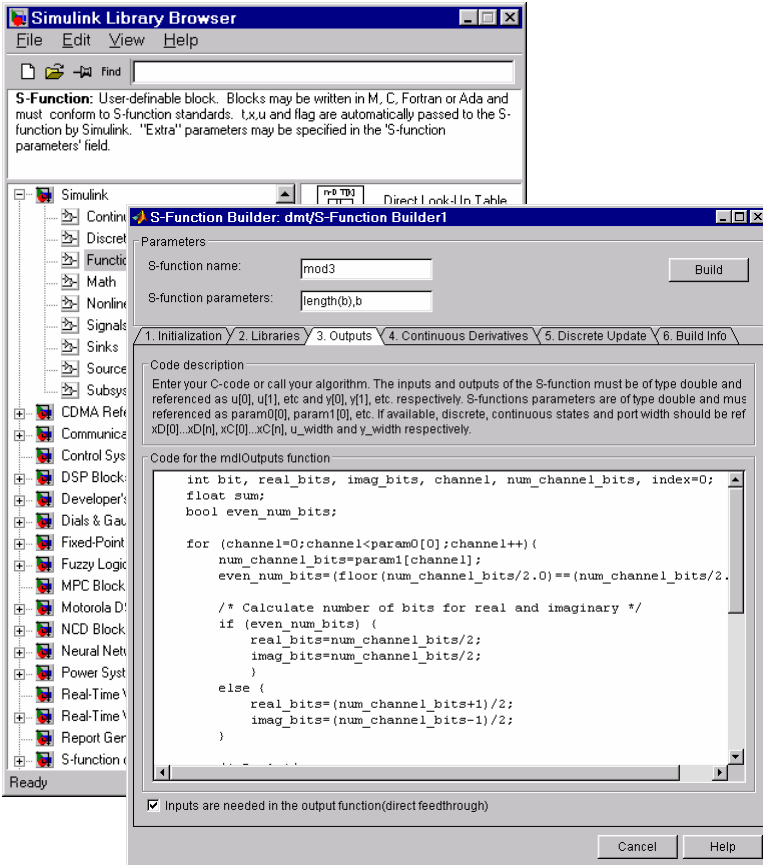
End-to-end systems

- Digital and analog operations such as coding, interleaving and modulation
- Channel models, error coding, sources, sinks
- Multiple rates for frames, symbols, bit and sample rates
- Synchronization
- Performance testing
- Analog, digital, hybrid, and event-driven simulation



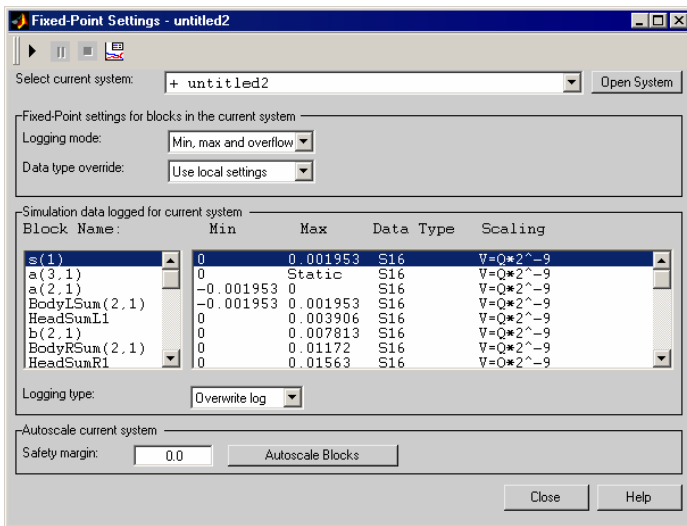
Co-develop with C Code

- S-function block in Simulink
 - API to specify outputs, state, parameters and sample-times
- S-function builder in Simulink
 - GUI to enter C Code
 - Predefined variables for input, output and states



Fixed Point Simulation

- New integrated fixed point in core Simulink (R13)
- User-definable data types
- Analysis tools
 - log min, max, overflows block-by-block
- Floating point override options



Fixed-Point Settings - untitled2

Select current system: + untitled2

Fixed-Point settings for blocks in the current system

Logging mode:

Data type override:

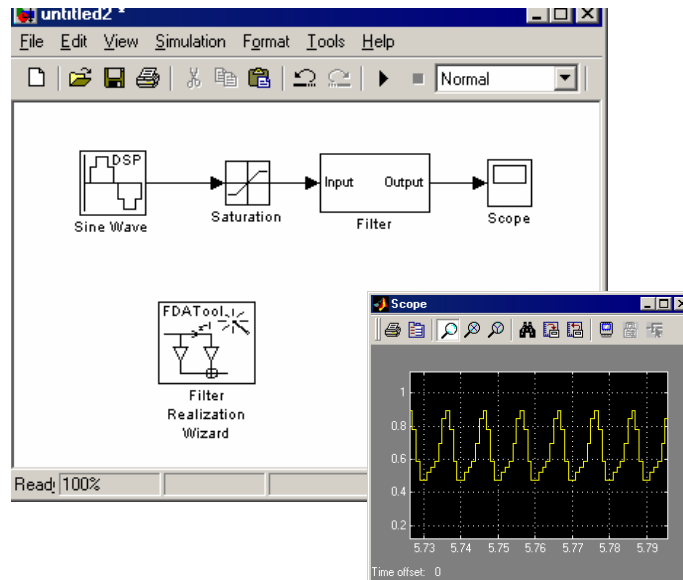
Simulation data logged for current system

Block Name:	Min	Max	Data Type	Scaling
s(1)	0	0.001953	S16	V=Q*2 ⁻⁹
a(3.1)	0	Static	S16	V=Q*2 ⁻⁹
a(2.1)	-0.001953	0	S16	V=Q*2 ⁻⁹
BodyISum(2.1)	-0.001953	0.001953	S16	V=Q*2 ⁻⁹
HeadSumL1	0	0.003906	S16	V=Q*2 ⁻⁹
b(2.1)	0	0.007813	S16	V=Q*2 ⁻⁹
BodyRSum(2.1)	0	0.01172	S16	V=Q*2 ⁻⁹
HeadSumR1	0	0.01563	S16	V=Q*2 ⁻⁹

Logging type:

Autoscale current system

Safety margin:



untitled2

File Edit View Simulation Format Tools Help

Normal

Sine Wave → Saturation → Input → Output → Scope

Filter Realization Wizard

Read: 100%

Scope

Time offset: 0

The Scope plot shows a signal waveform with a time axis from 5.73 to 5.79 and a vertical axis from 0.2 to 1.0.

Links to implementation

■ Real-Time Workshop

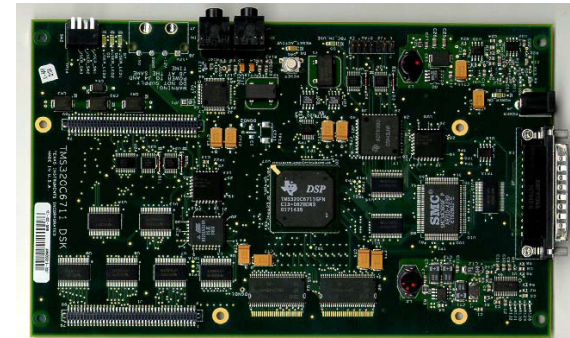
- Automatically generates ANSI C from Simulink
- Customizable code
- Rapid Prototyping

■ Embedded Targets

- TI C6000
- Motorola MPC555

■ Altera DSP Builder

- Bit-true and cycle-true Simulink library for common functions
- Automatic HDL code generation from a Simulink model
- Available from Altera



FIR Filter Design: demo

The image shows the MATLAB Filter Design & Analysis Tool (FDATool) interface. The main window displays the filter design process, including a block diagram on the left and a magnitude response plot on the right. The block diagram shows a signal path from a Signal Builder through a Filter block to an FFT block. The magnitude response plot shows the magnitude in dB versus normalized frequency, comparing the reference magnitude (blue line) and the quantized magnitude (green line). The plot shows a passband with ripples and a stopband with attenuation.

Filter response fixed vs floating

Select design algorithms

Filter specifications

Filter Design & Analysis Tool - [untitled.fda *]

File Edit Analysis Targets Window Help

Filter:

- Source: Imported
- Order: 20
- Stable: Yes
- Sections: 1

Filter Type:

- Lowpass

Filter Order:

- Specify order: 20
- Minimum order

Options:

- Minimum phase.
- Stopband slope (dB): 60
- Inverse sinc passband.

More options

Design Filter

Computing Response ... done.

untitled *

File Edit View Simulation Format Tools Help

Signal Builder

Signal 1

Input

Output

Filter

FFT

Spectrum Scope

FDATool Wizard

100%

FixedStepDiscrete

Magnitude Response

Magnitude Response in dB

Magnitude (dB)

Normalized Frequency ($\times\pi$ rad/sample)

Filter #1: Reference magnitude

Filter #1: Quantized magnitude

Filter Type

Filter Order

Options

Frequency Specifications

Magnitude Specifications

Units: MHz

Units: dB

Fs: 1.0833

Specify: passband edges

Asym: 0.01

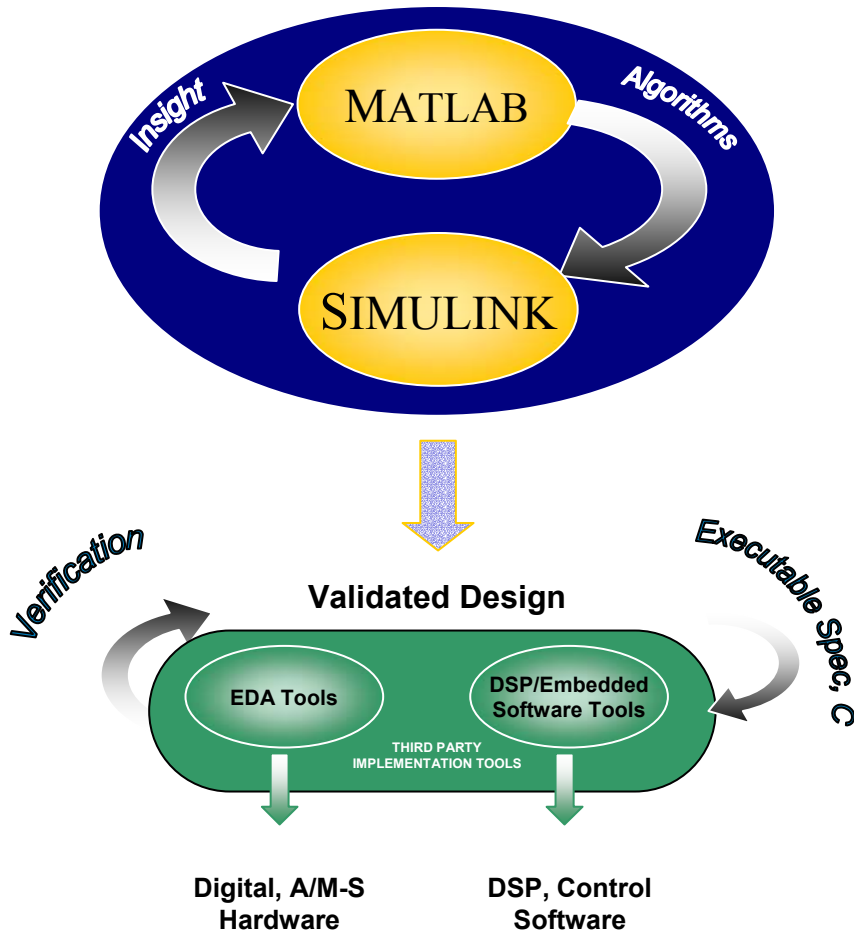


SOPC
WORLD
2 0 0 2



Summary

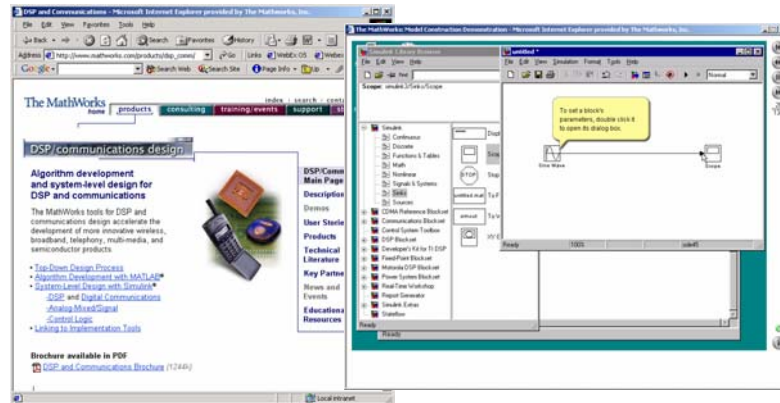
MATLAB and Simulink



- Create validated design
- Use as reference or executable specification to test low-level designs against
- Provide clear specifications
- Detect design flaws early
- Reduce risk and time-to-market

Further Information on Products and Services

- Product information and animated demonstrations
 - www.mathworks.com/products/dsp_comm
- Events
 - www.mathworks.com/dsp_events
 - Regular on-line software demonstrations



MATLAB Central

- www.mathworks.com/matlabcentral
- MathWorks and user contributed models

The left screenshot shows the MATLAB Central home page. It features the MATLAB Central logo and the text "file exchange and newsgroup access for the MATLAB & Simulink user community". Below this, there are sections for "file exchange" (a user-contributed code library) and "newsgroup access" (the MATLAB Usenet newsgroup). A "Recently added files..." section lists three files: PREPOSTIGUIS (Francesco di Piero), dashline (Edward Abraham), and CBNEEDLE (Steve Simon). A "Recently added posts..." section lists three posts: "Middle and right mouse button hits (1 message) - Tom Sweetland", "Plot in real time (1 message) - Sylvain Coanocan", and "weird problem?? (3 messages) - Chia C Chong".

The right screenshot shows a search results page for "Wireless Communications". It features a table of files with columns for Rating, Title, Submitted, and Downloads. The table lists three files:

Rating (5-highest)	Title	Submitted	Downloads
4 (1 reviewer)	RF Design and Analysis A collection of functions, scripts, & Simulink models useful for designing and analyzing RF systems Jackson Harvey	2001-07-23	4300
5 (3 reviewers)	Bluetooth modulation and frequency hopping Bluetooth modulation and frequency hopping Stuart McGarrity	2001-09-10	4029
4 (1 reviewer)	Bluetooth voice transmission Bluetooth Voice Transmission Stuart McGarrity	2001-10-09	2433

Below the table, there are sections for "Spotlight" (Arrows in the File Exchange), "Top Submissions" (RF Design and Analysis, Bluetooth modulation and frequency hopping, Bluetooth voice transmission, HiperLAN2 reference model, IS-95A Mobile Phone Call Processing), and "Top Download Lists" (Most Downloaded, Highest Rated, Top Authors, Most Recent).