AT17A Series Conversions from Altera FPGA Serial Configuration Memories

Introduction

The Atmel AT17A FPGA Configuration EEPROM (Configurator) is a serial memory that can be used to load SRAM based FPGAs. This application note describes use of the Atmel Configurator in place of the EPC1064, EPC1213, EPC1441, EPC1 and EPC2 devices when used with Altera FPGAs.

The Atmel Advantage

There are several advantages the Atmel Configurator provides, as shown in Table 1.

Having the ability to be In-System Programmed allows changes to designs without incurring the cost of an OTP device after each design modification. This translates into a reduction in development time, cost savings from flexible inventory control and easy field updates.

Memory Requirements

Memory requirements to program the Altera FLEX8000 series of FPGAs is shown in Table 2. The Atmel AT17A Series Configurators have a broader density offering than the Altera EPC family so a more efficient (smaller) Atmel memory can be used in several cases.

Table 1.

	Atmel AT17A	**Altera EPC**(1)
In-System Programmable (ISP)	Yes	No(3)
Reprogrammable	Yes	No(3)
3.3V Device Availability	Yes	Yes
3.3V In-System Programming	Yes	No(3)
8-pin DIP	Yes(5)	Yes(4)
20-pin PLCC	Yes(2)	Yes
Cascadable	Yes	Yes
Available as 128K x 1	Yes	No

Notes:
1. Source: Altera 1998 Databook (EPC1064, EPC1213, EPC1441 and EPC1 devices only.)
2. Atmel's 20-pin PLCC AT17A Series Configurators are directly pin-compatible with the EPC devices.
3. Reprogrammability limited to EPC2 device.
4. Not available for EPC2.
5. The Atmel AT17 family matches the Altera pinout for 8-pin DIP.

AT17A Series FPGA Configuration EEPROM Memory

Application Note

Rev. 0910B–10/99

Table 2. Altera FLEX8000 to Atmel Device Cross Reference

FLEX8000 Part Number	Configuration Bits	Altera OTP EPROM Part Number	Atmel ISP EEPROM Part Number
EPF8282	40K	EPC1064	AT17C/LV65(A)
EPF8452	64K	EPC1213	AT17C/LV65(A)
EPF8636	96K	EPC1213	AT17C/LV128(A)
EPF8820	128K	EPC1213	AT17C/LV128(A)
EPF81188	192K	EPC1213	AT17C/LV256(A)
EPF81500	250K	EPC1213 x 2	AT17C/LV256(A)

Note: 1. To order the 8-lead PDIP version refer to “FPGA Configuration EEPROM: 64K, 128K and 256K” (Doc. # 0391).

Table 3 shows the memory requirements to program the Altera FLEX10K series of FPGAs.

Table 3. Altera FLEX10K to Atmel Device Cross Reference

FLEX10K Part Number	Configuration Bits	Altera OTP EPROM Part Number	Atmel ISP EEPROM Part Number
EPF10K10	115K	EPC1441	AT17C/LV512A
EPF10K20	225K	EPC1441	AT17C/LV512A
EPF10K30	368K	EPC1441	AT17C/LV512A
EPF10K40	488K	EPC1	AT17C/LV512A
EPF10K50	609K	EPC1	AT17C/LV010A
EPF10K70	881K	EPC1	AT17C/LV010A
EPF10K100	1172K	EPC2 or EPC1 x 2	AT17C/LV020A or AT17C/LV010A x 2
EPF10K130	1563K	EPC2 or EPC1 x 2	AT17C/LV020A or AT17C/LV010A x 2
EPF10K200	TBD	EPC2 x 2 or EPC1 x 3	AT17C/LV020A x 2 or AT17C/LV010A x 3
EPF10K250	TBD	EPC2 x 2 or EPC1 x 4	AT17C/LV020A x 2 or AT17C/LV010A x 4

Note: 1. The EPC2 is only a 1,695,680 x 1-bit device; whereas, the AT17C/LV020A is a 2,097,152 x 1-bit (true 2M-bit) device.

For the Altera FLEX6K series of FPGAs, Table 4 shows the memory requirements for programming using Atmel AT17A Series Configurators.

Table 4. Altera FLEX6K to Atmel Device Cross Reference

FLEX6K Part Number	Configuration Bits	Altera OTP EPROM Part Number	Atmel ISP EEPROM Part Number
EPF6010	160K	EPC1441	AT17C/LV512A
EPF6016	260K	EPC1441	AT17C/LV512A
EPF6024	420K	EPC1441	AT17C/LV512A

Pin Compatibility (8-pin DIP)

The AT17 Series Configurators and the Altera EPC1064/EPC1213 parts are pin-compatible in the 8-pin DIP package.(1) Following correct device programming, the Atmel Configurator can be used in the EPC1064/EPC1213 socket directly without any printed circuit board modifications.

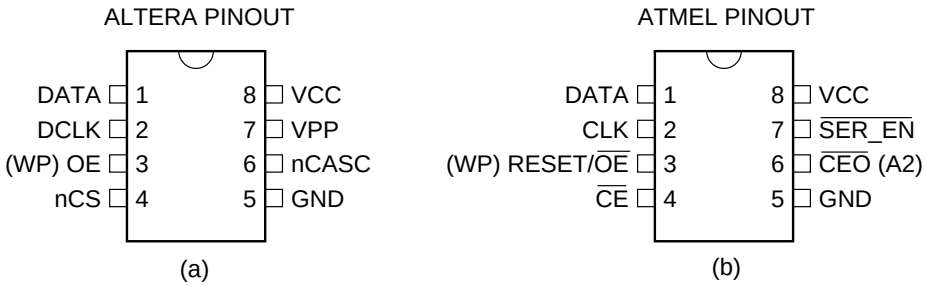
Table 5 shows the Atmel configurator pin name against the Altera device pin name. Figure 1 is a pictorial comparison of both 8-pin DIP packages.

Note: 1. To order the 8-lead PDIP version, refer to “FPGA Configuration EEPROM: 64K, 128K and 256K” (Doc # 0391).

Table 5. Pin Comparison 8-pin DIP

Device Pin Number	Altera 8-pin DIP Name	Atmel 8-pin DIP Name	Compatibility Notes
1	DATA	DATA	Pin-compatible
2	DCLK	CLK	Pin-compatible
3	(WP) OE	(WP) RESET/$\overline{OE}$	Pin-compatible when Reset polarity is programmed active Low (OE active High) in Atmel part
4	nCS	$\overline{CE}$	Pin-compatible
5	GND	GND	-
6	nCASC	$\overline{CEO}$ (A2)	Pin-compatible
7	VPP (programming pin)	$\overline{SER\_EN}$	OTP EPROM Programming pin used for ISP in AT17A Series Configurators
8	VCC	VCC	-

Figure 1. The (a) Altera 8-pin DIP and (b) AT17 8-pin DIP packages



Pin Compatibility (20-pin PLCC)

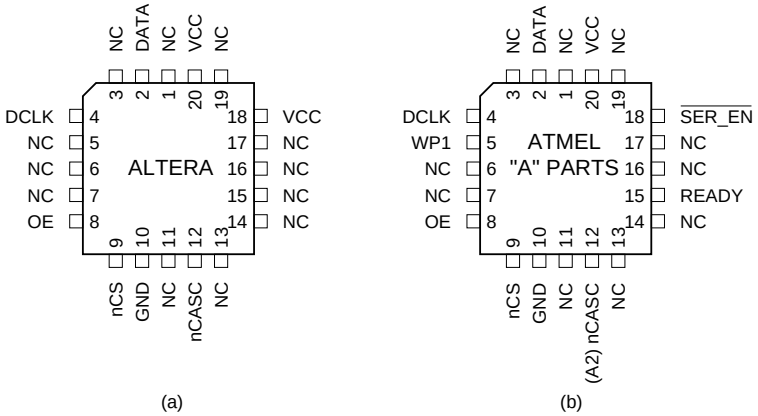
The AT17C020A/AT17C010A/AT17C512A are pin-compatible with the EPC2/EPC1/EPC1441 devices.

The AT17C65A/AT17C128A/AT17C256A are pin-compatible with the EPC1064/EPC1213 devices.

Table 6. Pin Comparison 20-pin PLCC

Device Pin Number	Altera 20-pin PLCC	Atmel 20-pin PLCC	Compatibility Notes
1	TDO	-	Optional feature in Altera EPC2 part
2	DATA	DATA	Pin-compatible
3	TCK	-	Optional feature in Altera EPC2 part
4	DCLK	DCLK	Pin-compatible
5	–	WP1	Optional feature in Atmel part 512A/010A
5	VCCSEL	-	Optional feature in Altera EPC2 part
8	OE	OE	Pin-compatible when reset polarity is programmed active Low (OE active High) in Atmel part
9	nCS	nCS	Pin-compatible
10	GND	GND	—
11	TDI	-	Optional feature in Altera EPC2 part
12	nCASC	nCASC (A2)	Pin-compatible
13	nINIT_CONF	-	Optional feature in Altera EPC2 part
14	VPPSEL	-	Optional feature in Altera EPC2 part
15	–	READY	Optional feature in Atmel part
18	VPP (programming pin)	$\overline{\text{SER\_EN}}$	OTP EPROM programming pin used for ISP in AT17A Series Configurators
19	TMS	-	Optional feature in Altera EPC2 part
20	VCC	VCC	—

Figure 2. The (a) Altera 20-pin PLCC and (b) AT17A Series 20-pin PLCC packages.



Notes:
1. AT17C/LV512A and AT17C/LV010A devices are only available in the 20-pin PLCC package outline.
2. The reset polarity of the Atmel device must be programmed active Low (OE active High) for use in Altera FPGA applications.
3. Altera pinout applies to EPC1/1441/1213/1064 and mandatory features of EPC2 only.
4. WP1 is available on AT17C512A/AT17C010A.

Replacing Altera's EPC OTP EPROMs with the AT17A Series Configuration EEPROMs

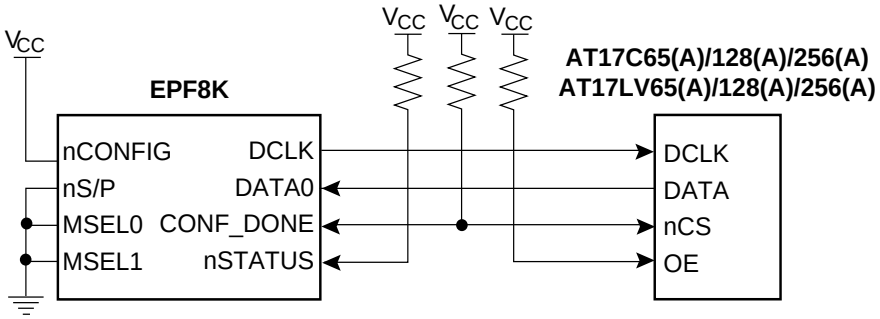
The Altera EPC devices can be replaced by Atmel AT17A Series Configuration EEPROMs by translating the Altera programming files for use with Atmel Configurator programming algorithms. To facilitate this process, Atmel provides a conversion utility, CPS (available free of charge from www.atmel.com), which supports Windows 95, Windows 98, and Windows NT operating systems. This software outputs an Intel (MCS-86) Hex file which can be read into industry-standard programmers. The software, in conjunction with Atmel's ATDH2200E Programming Kit, can be used to download an Altera programming file directly to Atmel Configurator(s).

Configurator Drop-in Applications

The AT17A Series Configurators can be used directly in Altera FPGA applications. The examples shown in the following pages demonstrate the ease with which Atmel Configurators can be used in place of Altera OTPs for the primary benefit of reprogrammability.

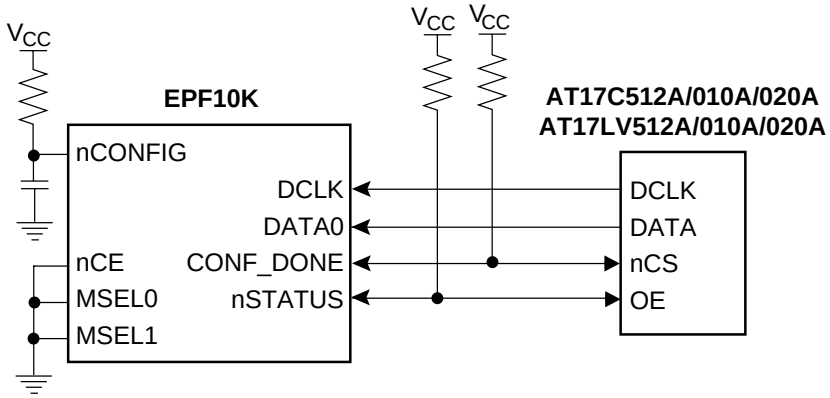
Each of the Drop-in Applications (Figure 3, Figure 4 and Figure 5) are similar to those corresponding to the use of the Altera OTP parts. Exceptions exist in Figure 4 and Figure 5, where an RC delay is recommended for use on the input to the nCONFIG pin; in order to emulate the 100 ms to 200 ms delay normally introduced on the DCLK line by the Altera OTP. This delay allows the system voltage to rise to within the normal operating range before allowing an FPGA configuration session.

Figure 3. Drop-in Replacement of the EPC1064/EPC1213 in an Altera FLEX8K Application



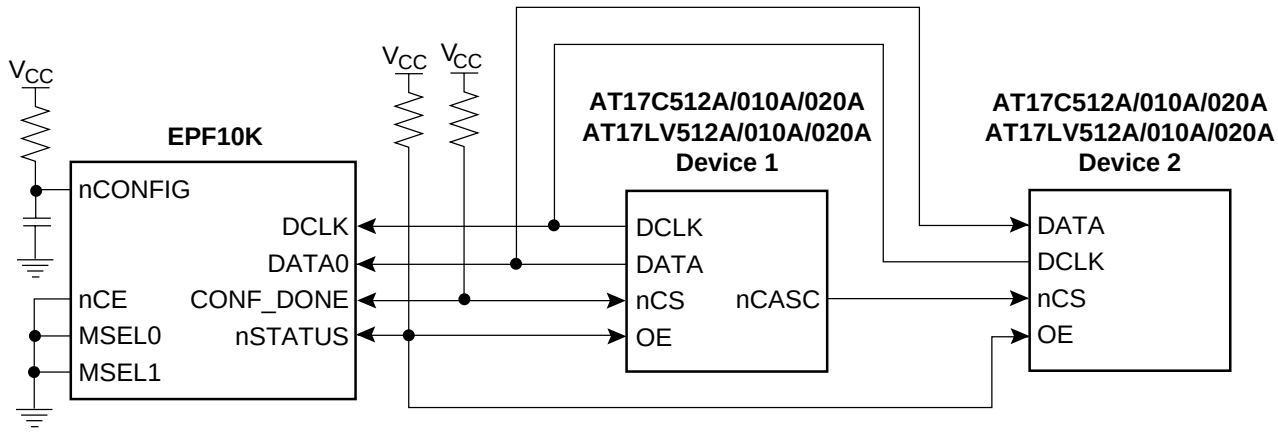
Notes: 1. 1.0 kΩ resistors used unless otherwise specified.
2. Reset polarity must be set active Low.

Figure 4. Drop-in Replacement of the EPC1441/EPC1/EPC2 in an Altera FLEX10K/6K Application



Notes: 1. 1.0 kΩ resistors used unless otherwise specified.
2. Applicable to EPF6K.
3. Reset polarity must be set active Low.
4. RC filter recommended for input to nCONFIG to delay configuration until VCC is stable. (nCONFIG can instead be connected to an active Low system reset signal.)

Figure 5. Drop-in Replacement of Cascaded EPC1441/EPC1/EPC2 OTPs in an Altera FLEX10K Application



Notes: 1. 1.0 kΩ resistors used unless otherwise specified.
2. Reset polarity must be set active Low.
3. RC filter recommended for input to nCONFIG to delay configuration until VCC is stable. (nCONFIG can instead be connected to an active Low system reset signal.)

In-System Programming Applications

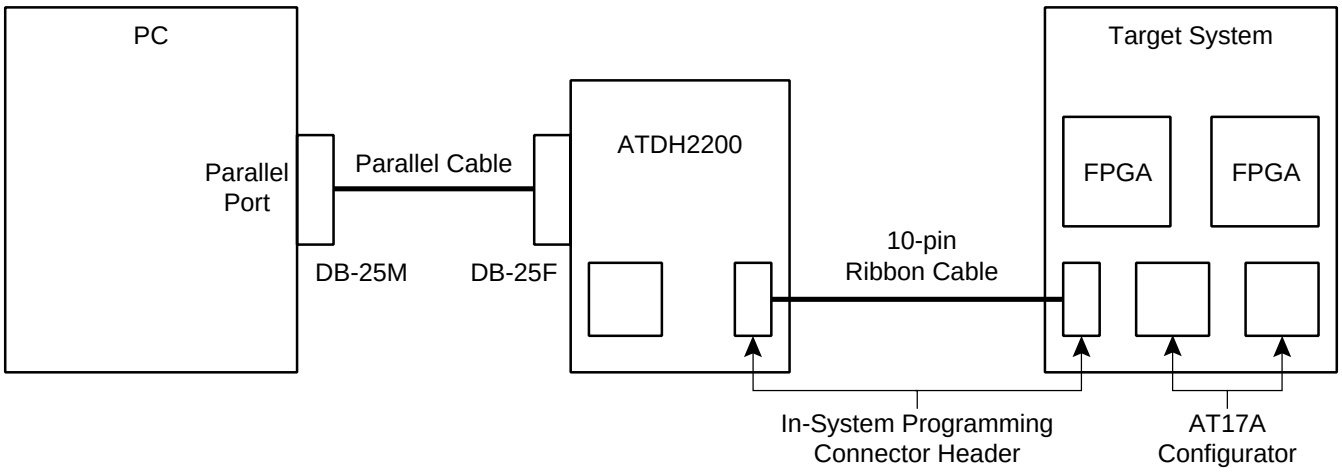
The AT17A Series Configurators are In-System (re)Programmable (ISP). The examples shown in the following pages support the following programmer functions:

1. Read the Manufacturers Code and the Device Code (512K and 1M parts only)
2. Program the device
3. Verify the device
4. Set the Reset Polarity option

While Atmel's FPGA Configurators can be programmed from various sources (e.g., on-board microcontrollers or PLDs), the applications shown here are designed to facilitate users of our ATDH2200 programming board and CF.exe download utility.

For in-system programming (ISP), the ATDH2200 board is used as a programming interface between the PC and the target board. Instead of populating the 17CXXX socket, the configurator(s) would be located on the target board. Communication to and from the configurator(s) would be accomplished via an ISP cable connected between the target board and the U7 header. File conversion and download is performed similar to the procedure described in the previous sections, but may require user intervention and additional chip select decoding circuitry/logic when targeting three or more devices on a given target board. The standard ISP system is shown below.

Figure 6. ATDH2200 ISP Programming Interface Board



Altera Applications

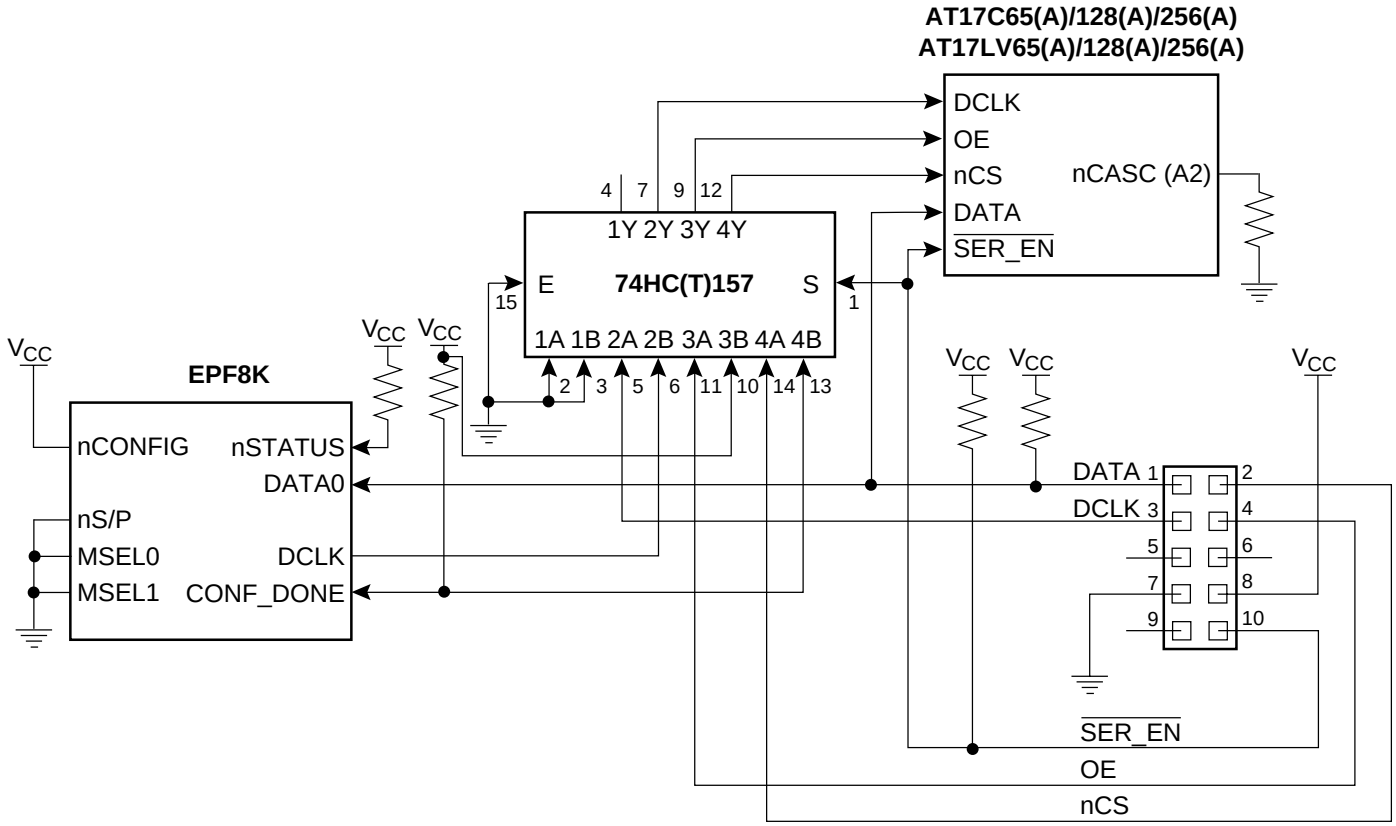
Altera FLEX devices (e.g., EPF10K, EPF6K, EPF8K) can be configured with any AT17A Series Configurators. However, high-density AT17A Series Configurators (512K and 1M-bit storage) introduce a simplified 3-wire interface that is highly desirable for ISP applications. For high-density or a-chained FPGAs, the AT17A Configurators can be cascaded to provide the necessary memory.

Figure 7 and Figure 8 employ the low-density AT17A Configurator for a single EPF8K and EPF6K device, respectively. The multiplexer IC (74HC(T)157) connects the configurator signals to either the FPGA or the ISP header.

The pull-down resistor on the A2 input pin of the configurator provides the required addressing for the incoming bitstream messages during programming. To target a specific configurator on the shared serial bus, the A2 bit from the programmer must match the level on the A2 input pin of the intended recipient. For users of Atmel's CF utility, the A2 bit can be modified using the /J <L | H> switch.

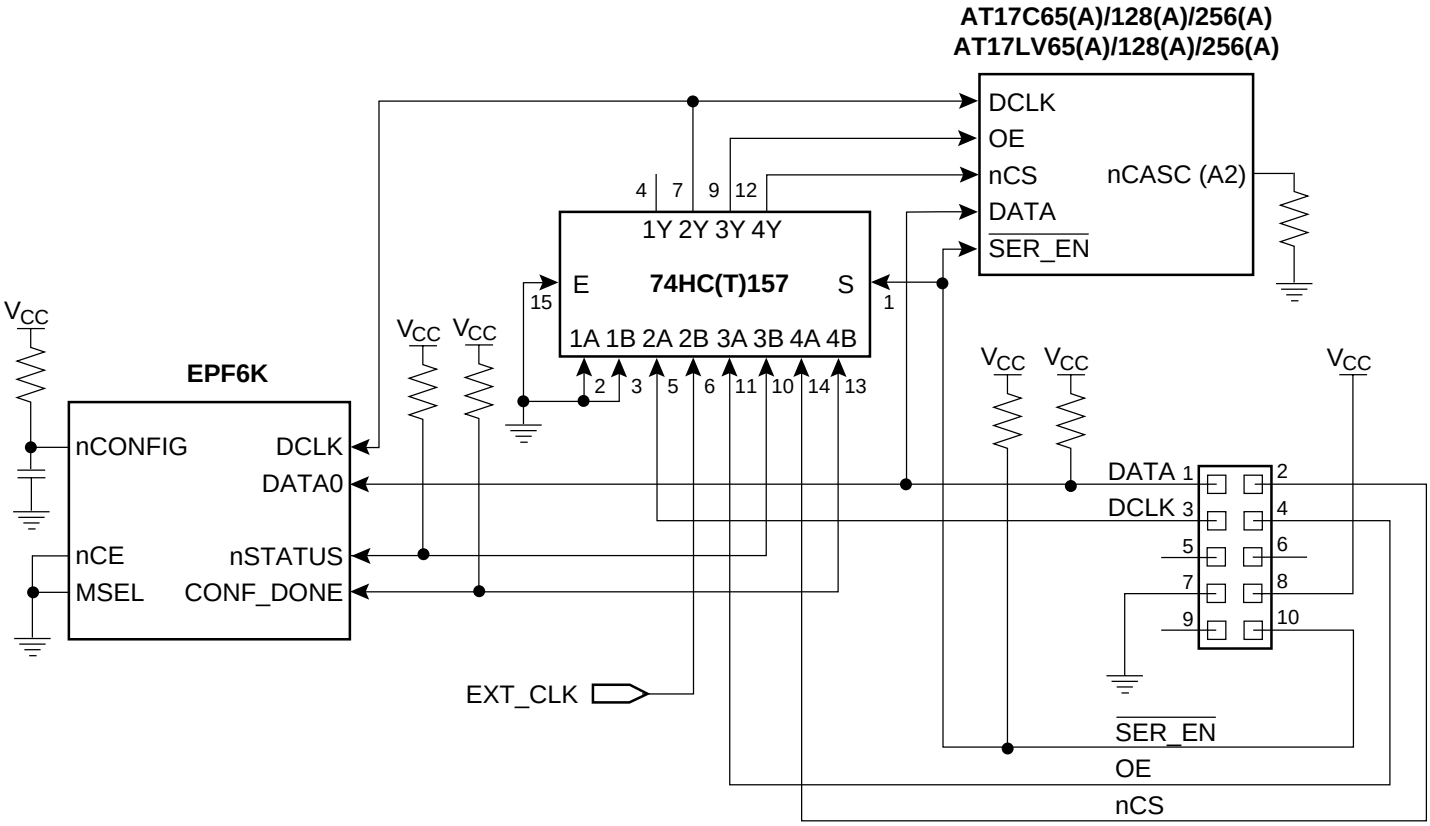
Next, $\overline{\text{SER\_EN}}$ serves as a control signal for the multiplexer select input and determines the operational mode of the EEPROM. For the low-density AT17A Configurators, control of the nCS and OE pins is necessary for the programming of user data and setting of the reset polarity.

Figure 7. ISP of the AT17C65(A)/128(A)/256(A) in an Altera FLEX8K Application



Notes: 1. 1.0 kΩ resistors used unless otherwise specified.
2. Reset polarity must be set active Low.

Figure 8. ISP of the AT17C65(A)/128(A)/256(A) in an Altera FLEX6K Application



Notes:
1. 1.0 kΩ resistors used unless otherwise specified.
2. Applicable to EPF10K.
3. Reset polarity must be set active low.
4. RC filter recommended for input to nCONFIG to delay configuration until VCC is stable. (nCONFIG can instead by connected to an active Low system reset signal.)

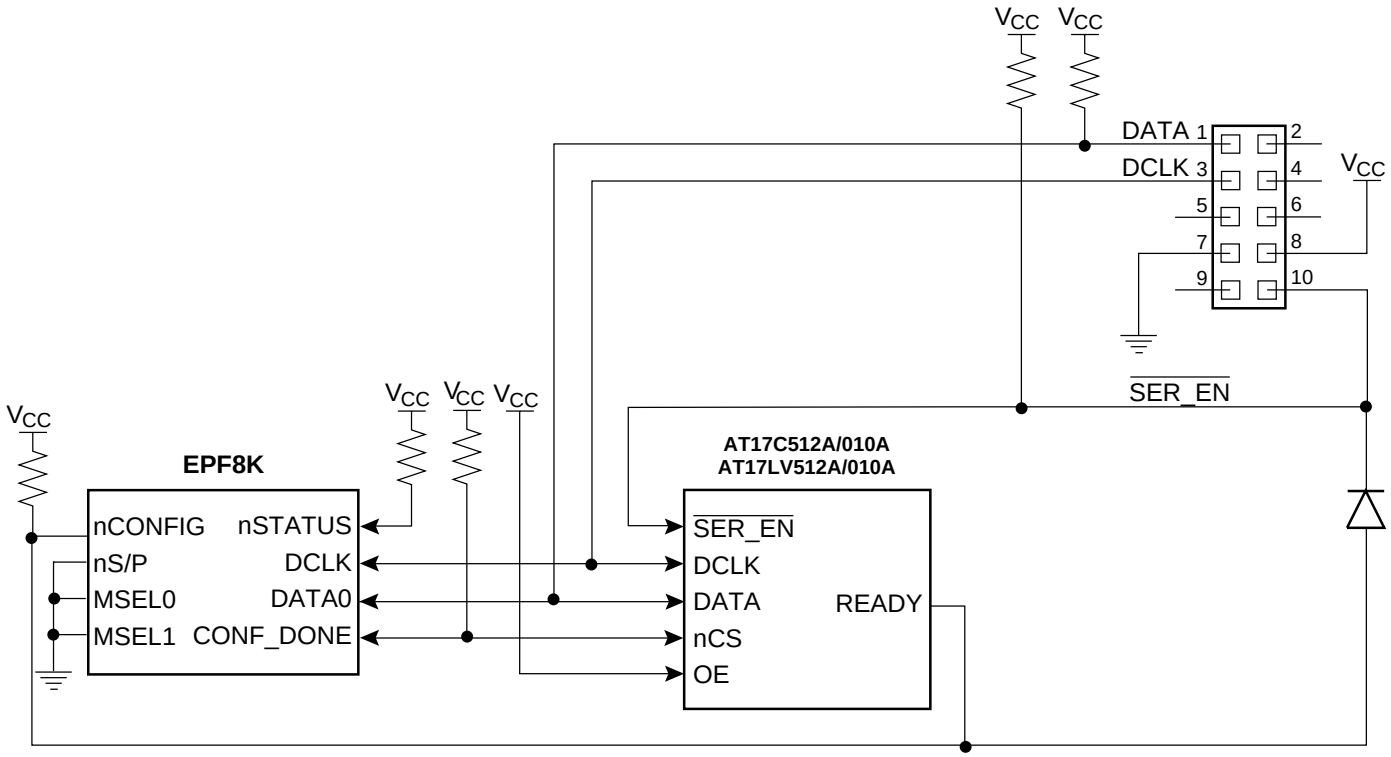
While the nCONFIG input pin can be connected directly to VCC, we recommend the use of an RC delay or connection to an active Low system reset signal for Altera FLEX10K/6K applications. This ensures that the VCC has entered into the normal operating levels prior to the start of configuration.

Since the low-density AT17A Series Configurators cannot provide the necessary clock signal (i.e. act as system master) during configuration, a clock must be supplied externally or from the FPGA.

The complexity of the ISP circuit is significantly reduced with the high-density AT17A Configurators as shown in Figure 9 and Figure 10. The diode connection between the EPF8K's nCONFIG pin and the $\overline{\text{SER\_EN}}$ signal allows the external programmer to force the FPGA into a reset state during ISP. This eliminates the potential for contention on the DCLK line. The READY pin (optional feature) of the configurator can also be connected to the FPGA's nCONFIG pin to force the FPGA to remain in a reset state as the configurator completes its power on reset cycle.

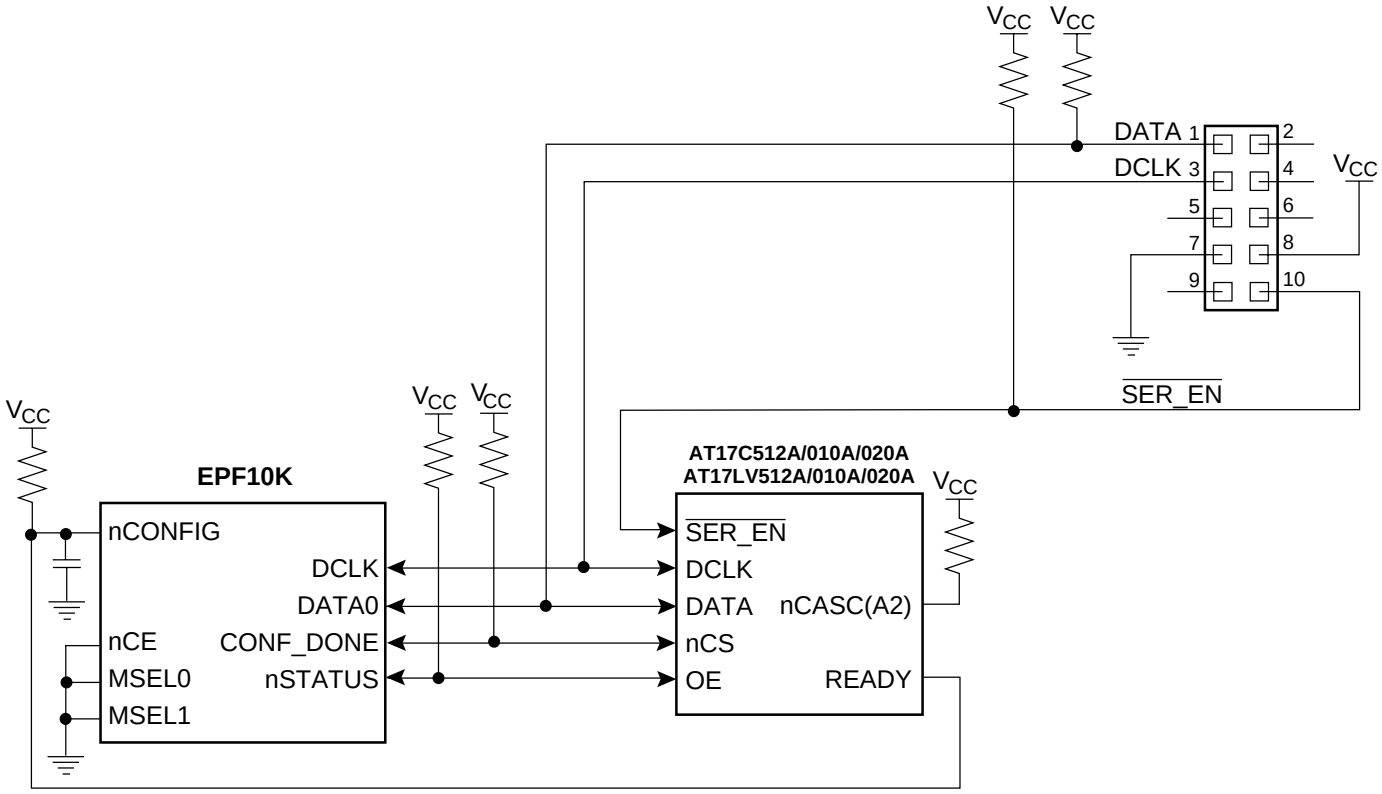
For the Altera FLEX8K application in Figure 9, the internal oscillator of the high-density AT17A Configurator must be disabled. This needs only to be performed once before device insertion, or during ISP by connecting nCS to the ISP header (not shown).

Figure 9. ISP of the AT17C512A/010A in an Altera FLEX8K Application



Notes:
1. 1.0 kΩ resistors used unless otherwise specified.
2. The internal oscillator of the AT17A Configurator is disabled.
3. Reset polarity must be set active Low.
4. Use of the READY pin is optional.

Figure 10. ISP of the AT17C512A/010A/020A in an Altera FLEX10K/6K Application



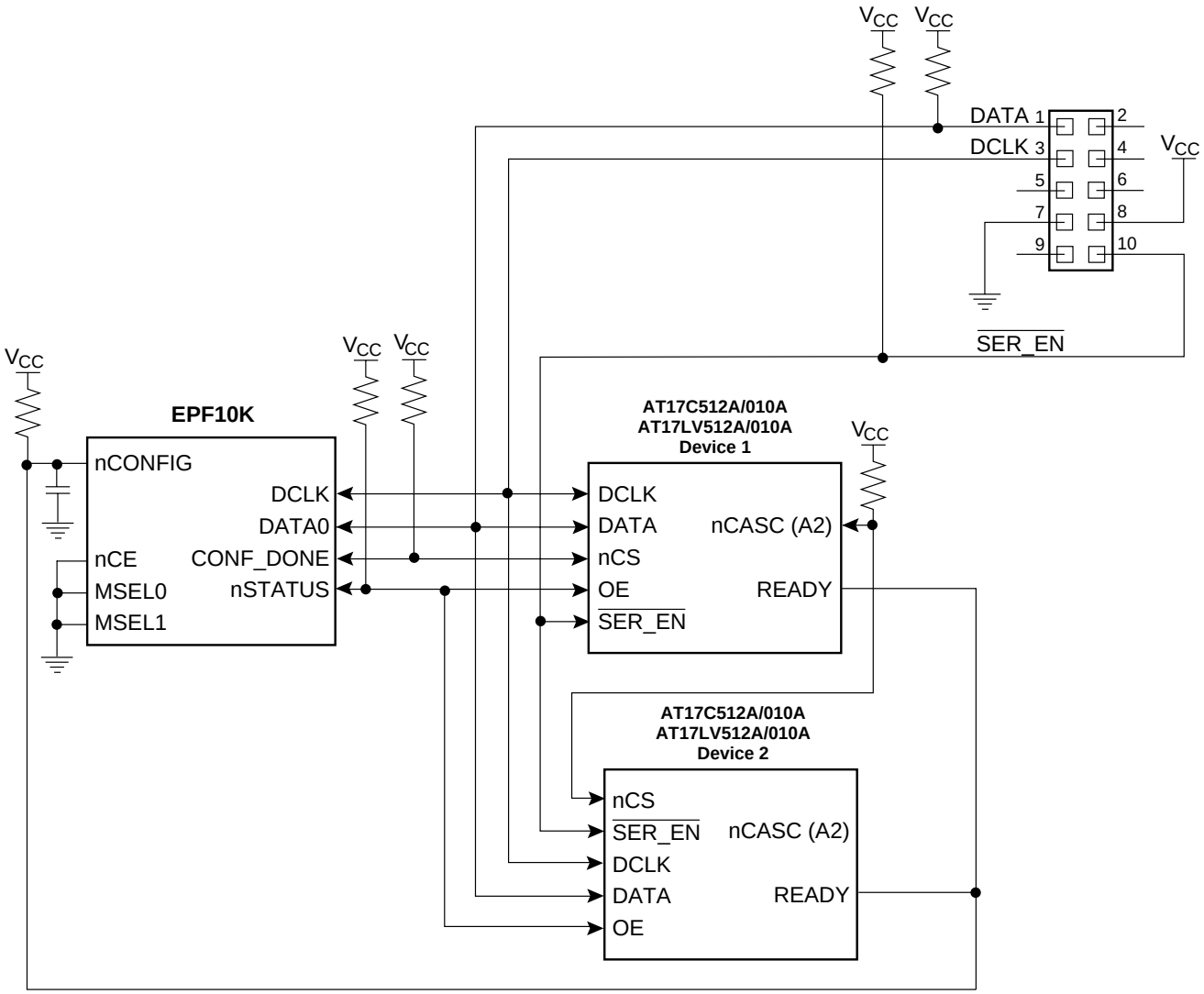
Notes:
1. 1.0 kΩ resistors used unless otherwise specified.
2. Applicable to EPF6K.
3. Reset polarity must be set active Low.
4. Use of the READY pin is optional.
5. RC filter recommended for input to nCONFIG to delay configuration until VCC is stable. (nCONFIG can instead be connected to an active Low system reset signal.)
6. The pull-up resistor on nCASC (A2) is required only for the AT17C/LV020A; it is otherwise optional.

The dedicated WP1 pin for the AT17C512A/010A if left unconnected, has a weak internal pull-down resistor that safely disables the write protection feature of these configurators. Similarly, an external pull-down resistor is not required on the A2 input during ISP since there is a weak internal pull-down resistor present on that pin.

In simple cascaded configurator applications involving two EEPROMs (Figure 11), the A2 input can be used as an addressing pin (set to logic level “0” for one EEPROM and logic level “1” for the other EEPROM). The programming utility can then modify the A2 bit sent in the bitstream messages to target either of the two EEPROMs.

Applications involving more than two EEPROMs must use the A2 input pin as a chip select. Pull-up resistors on each A2 input is required, in addition to an external decoder circuit which must be able to selectively drive each A2 input Low. For further details please refer to the Programming Cascaded Configurators application note.

Figure 11. ISP of Two Cascaded AT17C512A/010As in an Altera FLEX10K Application



Notes:
1. 1.0 kΩ resistors used unless otherwise specified.
2. Use of the READY pin is optional.
3. Reset polarity must be set active Low.
4. RC filter recommended for input to nCONFIG to delay configuration until VCC is stable. (nCONFIG can instead be connected to an active Low system reset signal.)
5. This circuit cannot be used with the AT17C/LV020A

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Application Support Hotline:
1-(408) 436-4119

e-mail:
configurator@atmel.com

FAQ:
Accessible from Web Site

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

0910B–10/99/xM