Includes FLEX 10KA

FLEX 10K

Embedded
Programmable Logic Family

May 2000, ver. 4.02

Data Sheet

Features…

- The industry's first embedded programmable logic device (PLD) family, providing System-on-a-Programmable-Chip™ integration
    - Embedded array for implementing megafunctions, such as efficient memory and specialized logic functions
    - Logic array for general logic functions
- High density
    - 10,000 to 250,000 typical gates (see Tables 1 and 2)
    - Up to 40,960 RAM bits; 2,048 bits per embedded array block (EAB), all of which can be used without reducing logic capacity
- System-level features
    - MultiVolt™ I/O interface support
    - 5.0-V tolerant input pins in FLEX® 10KA devices
    - Low power consumption (typical specification less than 0.5 mA in standby mode for most devices)
    - FLEX 10K and FLEX 10KA devices support peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*
    - FLEX 10KA devices include pull-up clamping diode, selectable on a pin-by-pin basis for 3.3-V PCI compliance
    - Select FLEX 10KA devices support 5.0-V PCI buses with eight or fewer loads
    - Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990, available without consuming any device logic

Table 1. FLEX 10K Device Features

Feature	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
Typical gates (logic and RAM) (1)	10,000	20,000	30,000	40,000	50,000
Maximum system gates	31,000	63,000	69,000	93,000	116,000
Logic elements (LEs)	576	1,152	1,728	2,304	2,880
Logic array blocks (LABs)	72	144	216	288	360
Embedded array blocks (EABs)	3	6	6	8	10
Total RAM bits	6,144	12,288	12,288	16,384	20,480
Maximum user I/O pins	150	189	246	189	310

Table 2. FLEX 10K Device Features

Feature	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
Typical gates (logic and RAM) (1)	70,000	100,000	130,000	250,000
Maximum system gates	118,000	158,000	211,000	310,000
LEs	3,744	4,992	6,656	12,160
LABs	468	624	832	1,520
EABs	9	12	16	20
Total RAM bits	18,432	24,576	32,768	40,960
Maximum user I/O pins	358	406	470	470

Note to tables:
(1)   The embedded IEEE Std. 1149.1 JTAG circuitry adds up to 31,250 gates in addition to the listed typical or maximum system gates.

...and More Features

- Devices are fabricated on advanced processes and operate with a 3.3-V or 5.0-V supply voltage (see Table 3)
- In-circuit reconfigurability (ICR) via external configuration device, intelligent controller, or JTAG port
- ClockLock™ and ClockBoost™ options for reduced clock delay/skew and clock multiplication
- Built-in low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required

Table 3. Supply Voltages for FLEX 10K & FLEX 10KA Devices

5.0-V Devices	3.3-V Devices
EPF10K10	EPF10K10A
EPF10K20	EPF10K30A
EPF10K30	EPF10K50V
EPF10K40	EPF10K100A
EPF10K50	EPF10K130V
EPF10K70	EPF10K250A
EPF10K100	

■ Flexible interconnect
- FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
- Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
- Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
- Tri-state emulation that implements internal tri-state buses
- Up to six global clock signals and four global clear signals
■ Powerful I/O pins
- Individual tri-state output enable control for each pin
- Open-drain option on each I/O pin
- Programmable output slew-rate control to reduce switching noise
- FLEX 10KA devices support hot-socketing
■ Peripheral register for fast setup and clock-to-output delay
■ Flexible package options
- Available in a variety of packages with 84 to 600 pins (see Table 4)
- Pin-compatibility with other FLEX 10K devices in the same package
- FineLine BGA™ packages maximize board space efficiency
■ Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations, and Quartus™ development system for Windows-based PCs and Sun SPARCstation and HP 9000 Series 700 workstations
■ Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 4. FLEX 10K PLCC, TQFP, PQFP, RQFP & PGA Package Options & I/O Pin Count *Notes (1), (2)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	403-Pin PGA
EPF10K10	59		102	134		
EPF10K10A		66	102	134		
EPF10K20			102	147	189	
EPF10K30				147	189	
EPF10K30A			102	147	189	
EPF10K40				147	189	
EPF10K50					189	310
EPF10K50V					189	
EPF10K70					189	
EPF10K100						
EPF10K100A					189	
EPF10K130V						
EPF10K250A						

Table 5. FLEX 10K BGA & FineLine BGA Package Options & I/O Pin Count *Notes (1), (2)*

Device	503-Pin PGA	599-Pin PGA	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	600-Pin BGA
EPF10K10						
EPF10K10A			150		150 *(3)*	
EPF10K20						
EPF10K30				246		
EPF10K30A			191	246	246	
EPF10K40						
EPF10K50				274		
EPF10K50V				274	291	
EPF10K70	358					
EPF10K100	406					
EPF10K100A				274	369	406
EPF10K130V		470				470
EPF10K250A		470				470

Notes to tables:

(1)   Contact Altera Customer Marketing for up-to-date information on package availability.

(2)   FLEX 10K and FLEX 10KA device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), pin-grid array (PGA), and FineLine BGA™ packages.

(3)   This option will be supported with a 256-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin compatible. For example, a board can be designed to support both 256-pin and 484-pin FineLine BGA packages. The Quartus and MAX+PLUS II software automatically avoids conflicting pins when future migration is set.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10K devices are reconfigurable, which allows 100% testing prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Additionally, the designer does not need to manage inventories of different ASIC designs; FLEX 10K devices can be configured on the board for the specific functionality required.

Table 6 shows FLEX 10K performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. No special design technique was required to implement the applications; the designer simply inferred or instantiated a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 6. FLEX 10K & FLEX 10KA Performance

Application	Resources Used		Performance				Units
			Speed Grade				
	LEs	EABs	-1	-2	-3	-4	
16-bit loadable counter *(1)*	16	0	204	166	125	95	MHz
16-bit accumulator *(1)*	16	0	204	166	125	95	MHz
16-to-1 multiplexer *(2)*	10	0	4.2	5.8	6.0	7.0	ns
256 × 8 RAM read cycle speed *(3)*	0	1	172	145	108	84	MHz
256 × 8 RAM write cycle speed *(3)*	0	1	106	89	68	63	MHz

Notes:

(1)   The speed grade of this application is limited because of clock high and low specifications.

(2)   This application uses combinatorial inputs and outputs.

(3)   This application uses registered inputs and outputs.

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The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, embedded megafunctions typically cannot be customized, limiting the designer's options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC2, EPC1, and EPC1441 configuration devices, which configure FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera's BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, or ByteBlasterMV™ parallel port download cable (the ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program or configure 2.5-V, 3.3-V, and 5.0-V devices). After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 320 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized interface that permits microprocessors to configure FLEX 10K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

For more information, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlaster Parallel Port Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 59 (Configuring FLEX 10K Devices)*

FLEX 10K devices are supported by Quartus and MAX+PLUS II development systems; a single, integrated package that offers schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Quartus and MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Quartus and MAX+PLUS II software works easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Quartus and MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Quartus and MAX+PLUS II development systems include DesignWare functions that are optimized for the FLEX 10K architecture.

The MAX+PLUS II development system runs on Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations, and the Quartus development system runs on Windows-based PCs and Sun SPARCstation and HP 9000 Series 700 workstations.

See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* for more information.

Functional Description

Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10K devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 1.6 ns and hold times of 0 ns; as outputs, these registers provide clock-to-output times as low as 5.3 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the FLEX 10K architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each row and column of the FastTrack Interconnect.

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Figure 1. FLEX 10K Device Block Diagram
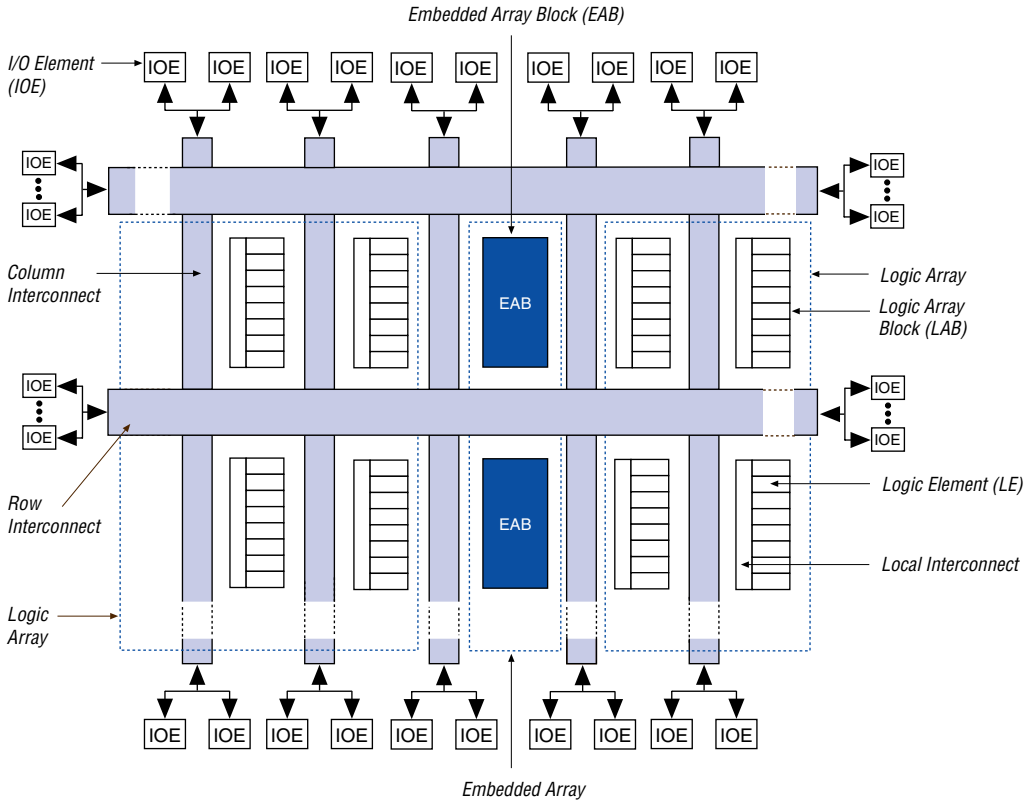
FLEX 10K devices provide six dedicated inputs that drive the flipflops' control inputs to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits, because it is large and flexible. These functions can be combined in applications such as digital filters and microcontrollers.

Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 4×4 multiplier with eight inputs and eight outputs. Parameterized functions such as LPM functions can automatically take advantage of the EAB.

The EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the EAB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

When used as RAM, each EAB can be configured in any of the following sizes: 256×8, 512×4, $1,024 \times 2$, or $2,048 \times 1$. See Figure 2.

Figure 2. EAB Memory Configurations

256×8 512×4 $1,024 \times 2$ $2,048 \times 1$

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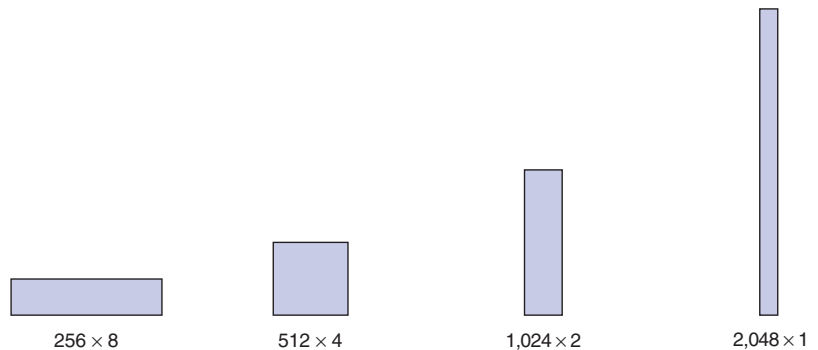
Larger blocks of RAM are created by combining multiple EABs. For example, two 256×8 RAM blocks can be combined to form a 256×16 RAM block; two 512×4 blocks of RAM can be combined to form a 512×8 RAM block. See Figure 3.

Figure 3. Examples of Combining EABs
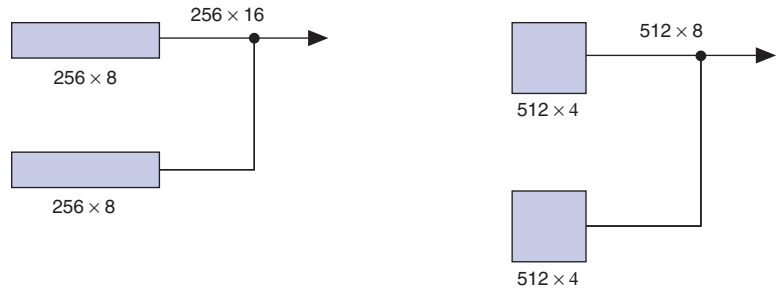
If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's MAX+PLUS II software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and WE inputs. The global signals and the EAB local interconnect can drive the WE signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the WE signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See Figure 4.

Figure 4. FLEX 10K Embedded Array Block
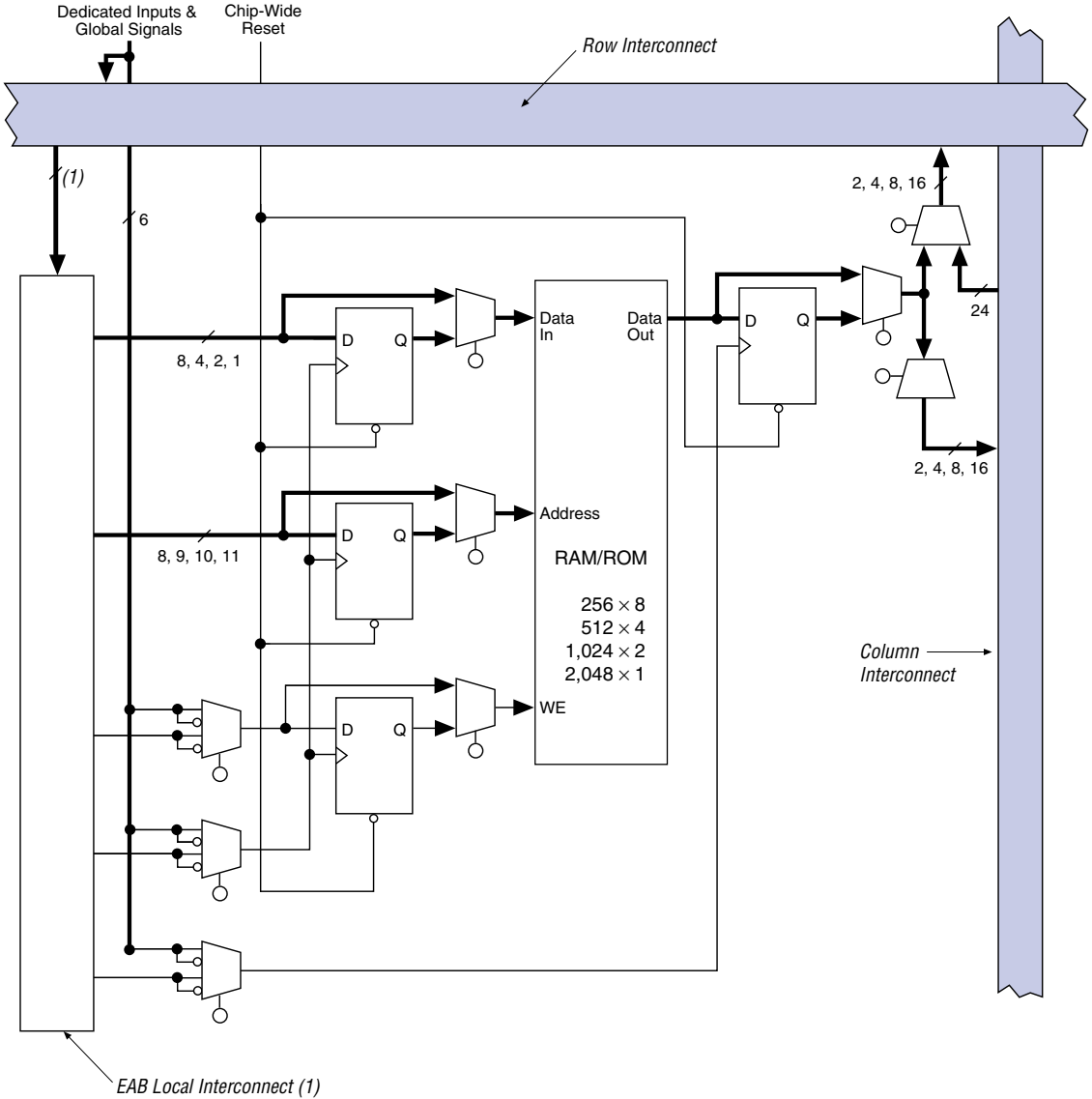
Note:

(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 EAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

Logic Array Block

Each LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10K architecture, facilitating efficient routing with optimum device utilization and high performance. See Figure 5.

Figure 5. FLEX 10K LAB
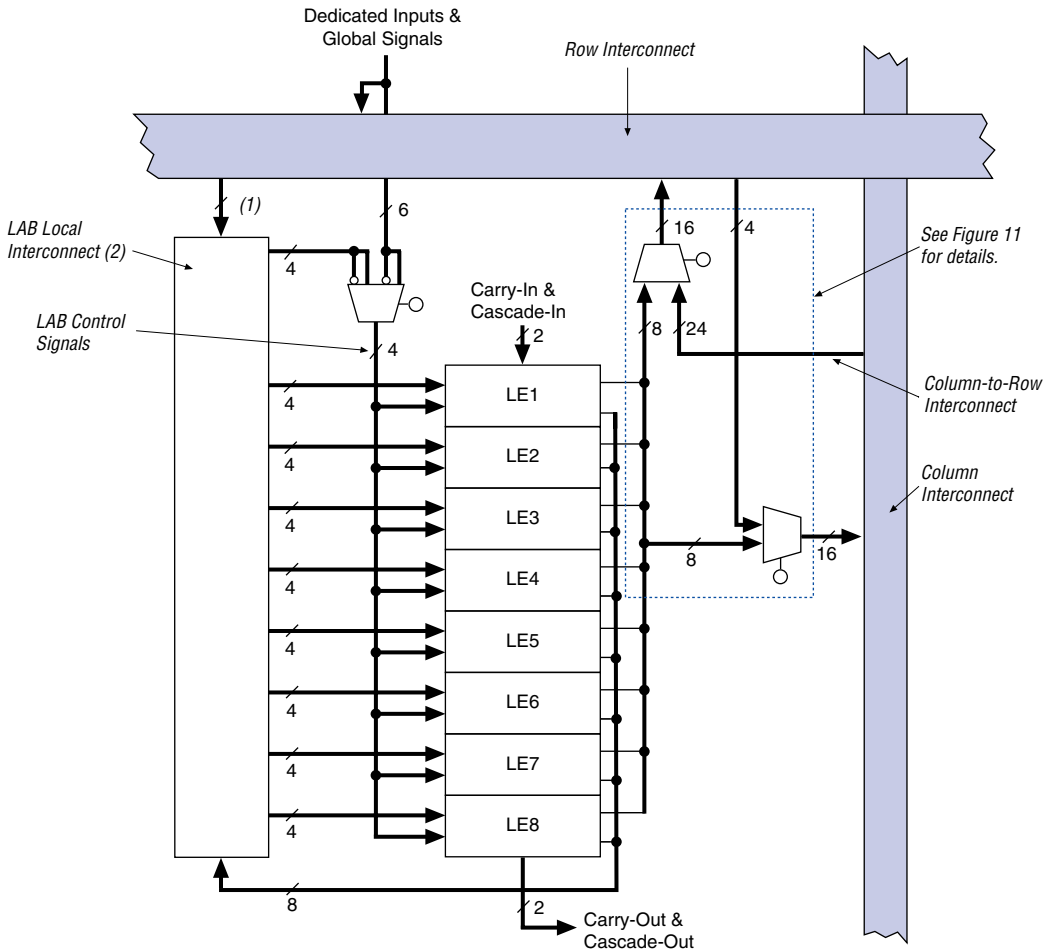
Notes:
(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.
(2) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 30 LAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 34 LABs.

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Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

Figure 6. FLEX 10K Logic Element
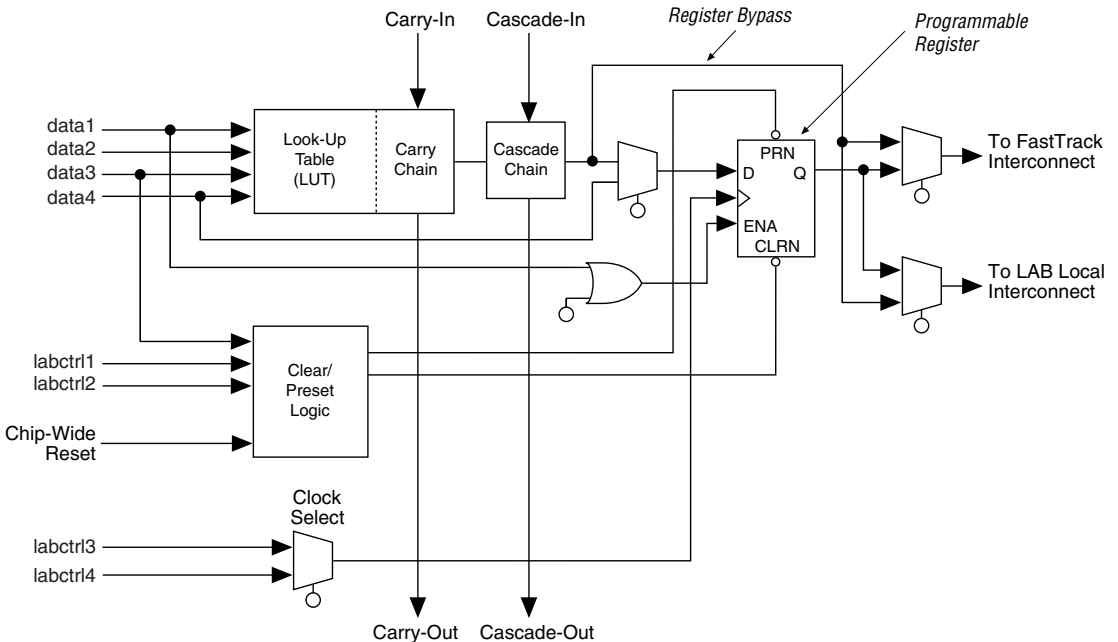
The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The FLEX 10K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10K architecture to implement high-speed counters, adders, and comparators of arbitrary width efficiently. Carry chain logic can be created automatically by the Quartus and MAX+PLUS II Compilers during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EPF10K50 device, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

Figure 7 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can either be bypassed for simple adders or be used for an accumulator function. The carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 7. Carry Chain Operation (n-bit Full Adder)
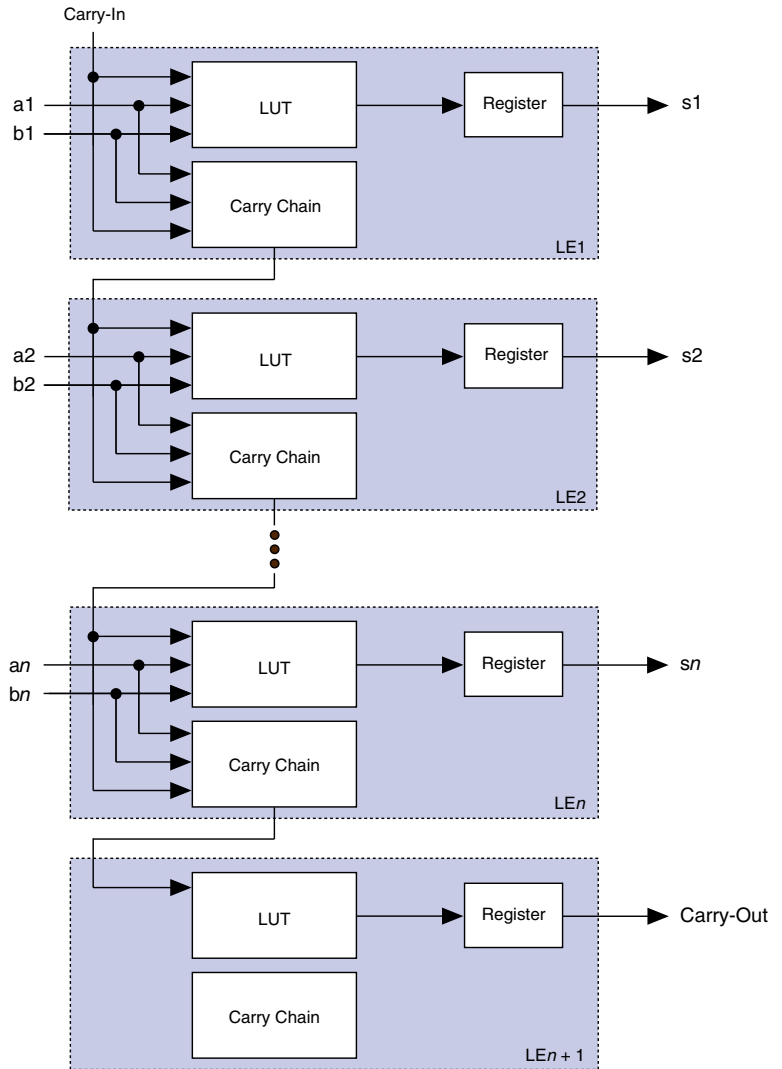
Cascade Chain

With the cascade chain, the FLEX 10K architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.7 ns per LE. Cascade chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EPF10K50 device, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 8 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. The LE delay is as low as 1.6 ns; the cascade chain delay is as low as 0.7 ns. With the cascade chain, 3.7 ns is needed to decode a 16-bit address.

Figure 8. Cascade Chain Operation

AND Cascade Chain

OR Cascade Chain

d[3..0]   LUT   LE1

d[7..4]   LUT   LE2

d[(4*n*-1)..(4*n*-4)]   LUT   LE*n*

d[3..0]   LUT   LE1

d[7..4]   LUT   LE2

d[(4*n*-1)..(4*n*-4)]   LUT   LE*n*
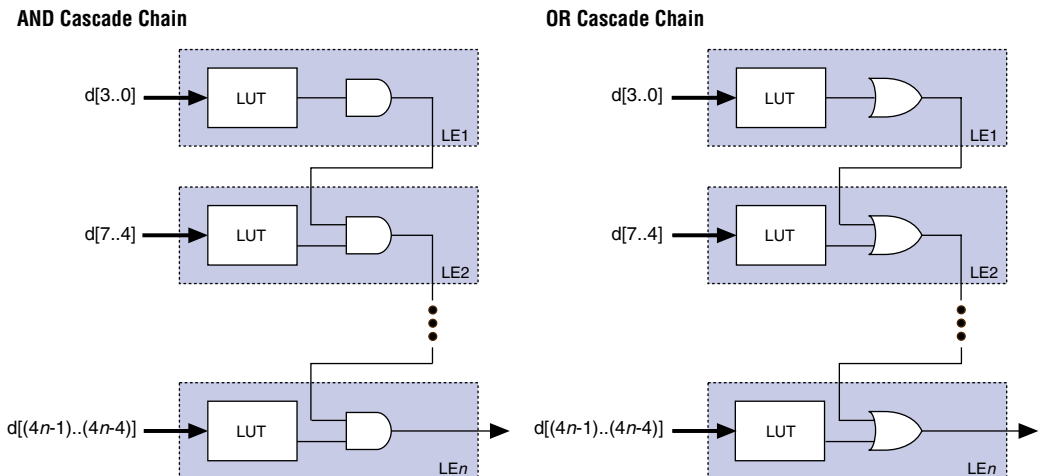
LE Operating Modes

The FLEX 10K LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. Quartus and MAX+PLUS II software packages, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions which use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. Quartus and MAX+PLUS II software packages can set DATA1 to enable the register synchronously, providing easy implementation of fully synchronous designs.

Figure 9 shows the LE operating modes.

Figure 9. FLEX 10K LE Operating Modes

Normal Mode
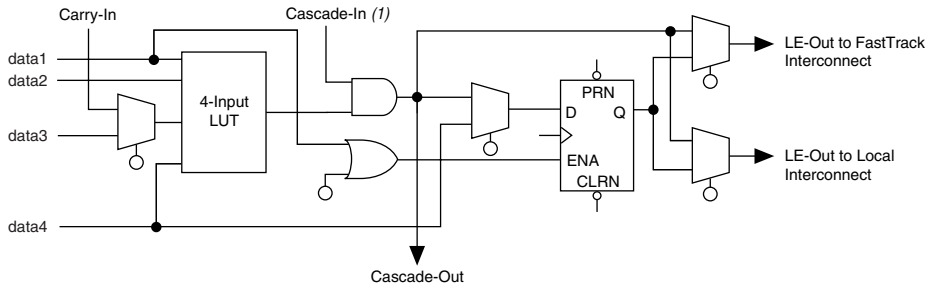
Arithmetic Mode
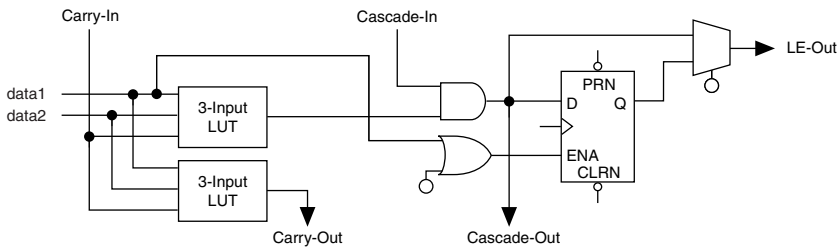
Up/Down Counter Mode
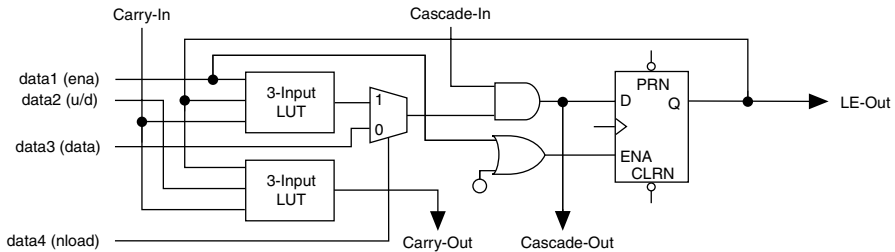
Clearable Counter Mode
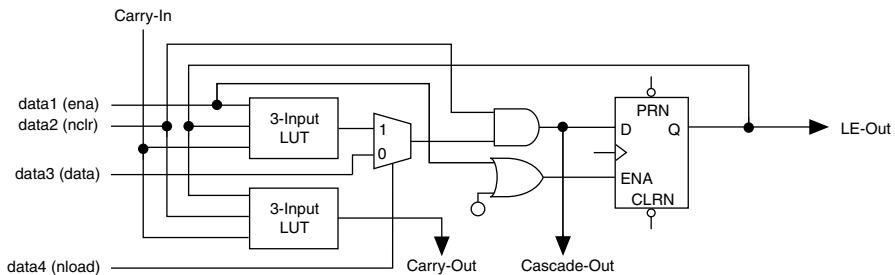
Note:

(1) Packed registers cannot be used with the cascade chain.

Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time.

The LUT and the register in the LE can be used independently; this feature is known as register packing. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a 3-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a 4-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a 3-input function, and the other generates a carry output. As shown in Figure 9 on page 19, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

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Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Quartus and MAX+PLUS II Compilers automatically select the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 10 shows examples of how to enter a section of a design for the desired functionality.

Figure 10. LE Clear & Preset Modes
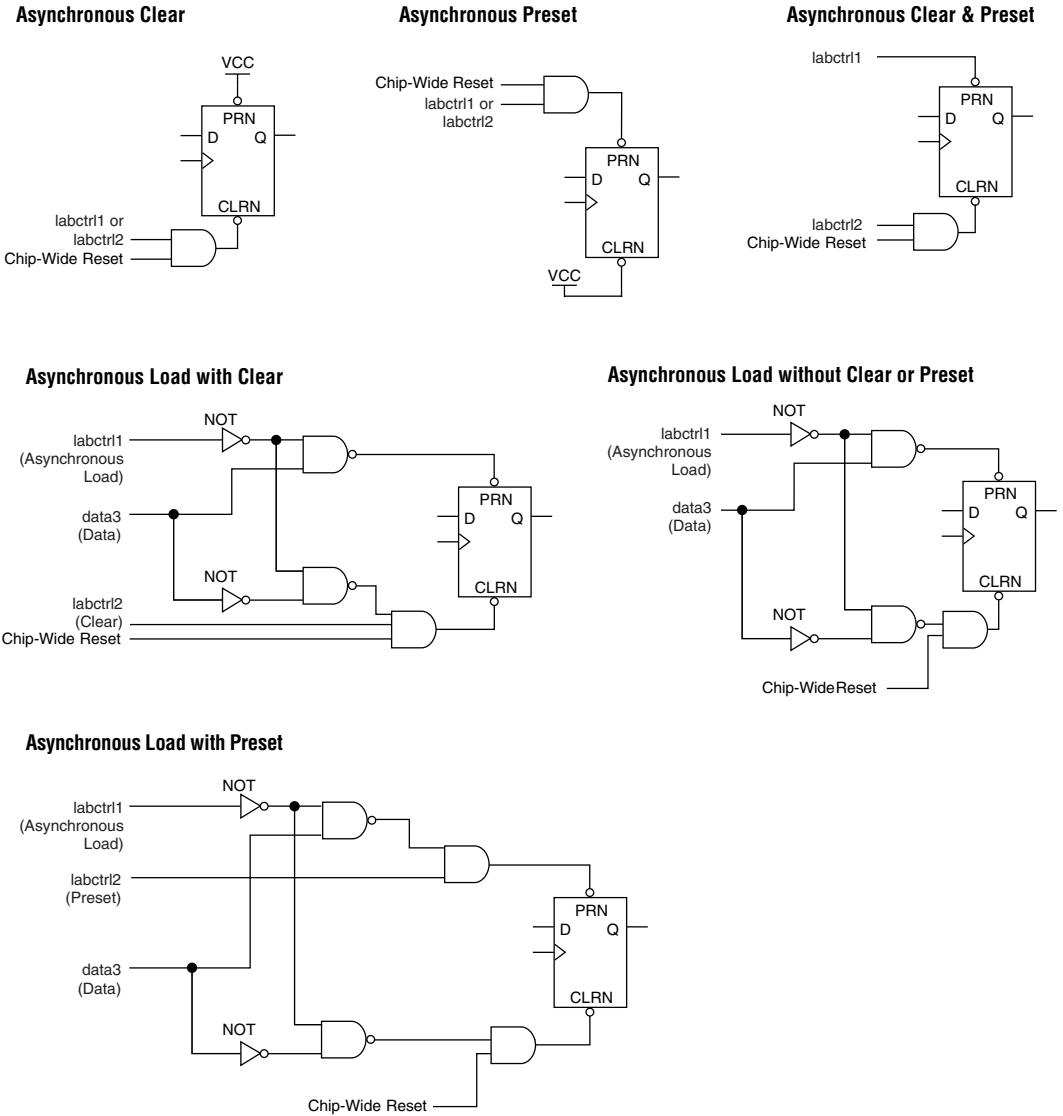
Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to V_{CC} to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to V_{CC}, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to V_{CC}, therefore, asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The MAX+PLUS II software inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

FastTrack Interconnect

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the device. The column interconnect routes signals between rows and can drive I/O pins.

A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in an LAB drive the row interconnect.

Each column of LABs is served by a dedicated column interconnect. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must be routed to the row interconnect before it can enter an LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, an LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently. See Figure 11.

Figure 11. LAB Connections to Row & Column Interconnect

Column
Channels

Row Channels

To Other
Columns

At each intersection,
four row channels can
drive column channels.

Each LE can drive two
row channels.

From Adjacent LAB
To Adjacent LAB

LE 1

LE 2

LE 8

Each LE can switch
interconnect access
with an LE in the
adjacent LAB.

To LAB Local
Interconnect

To Other Rows
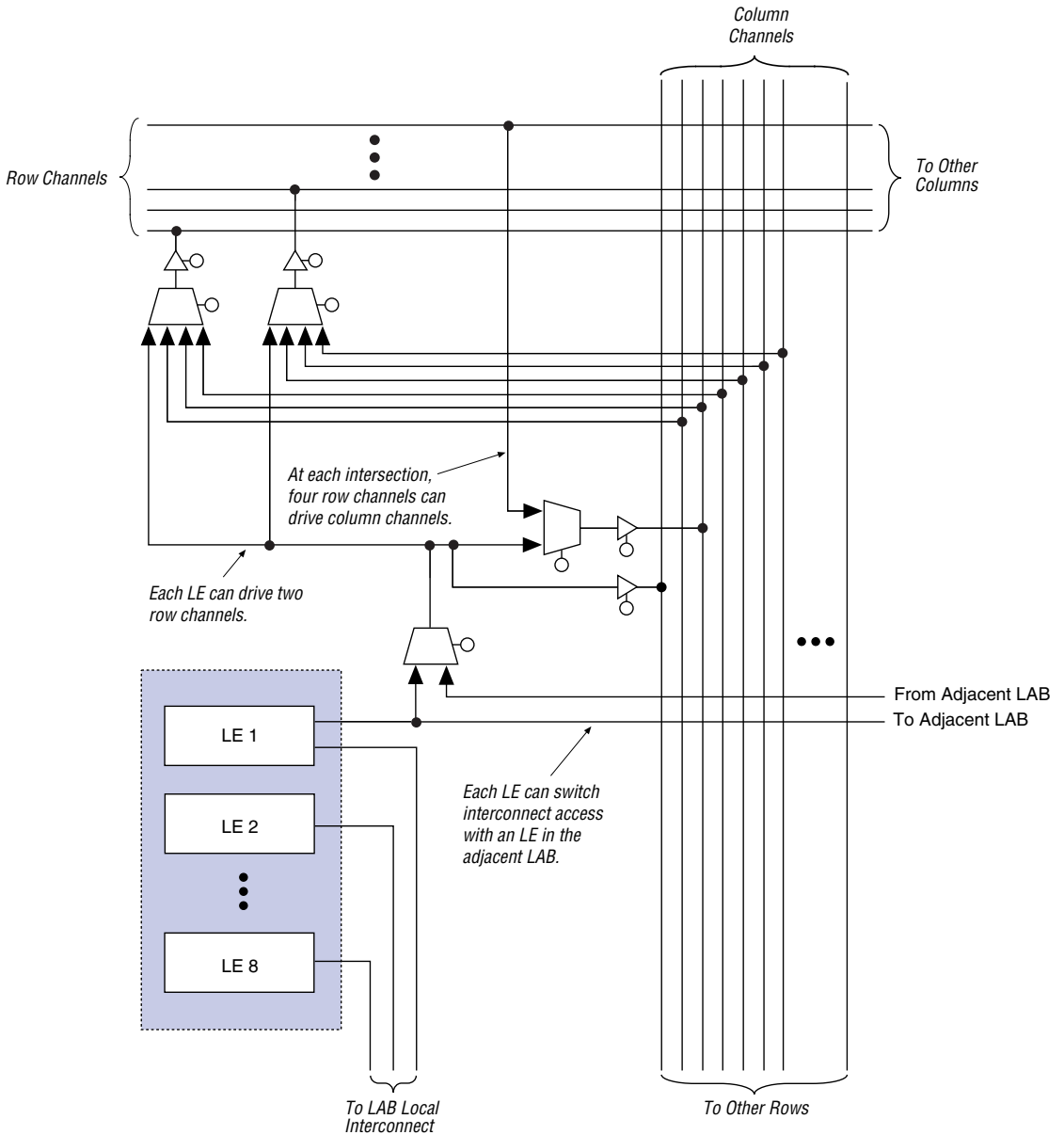
For improved routing, the row interconnect is comprised of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 7 summarizes the FastTrack Interconnect resources available in each FLEX 10K device.

Table 7. FLEX 10K FastTrack Interconnect Resources				
Device	**Rows**	**Channels per Row**	**Columns**	**Channels per Column**
EPF10K10 EPF10K10A	3	144	24	24
EPF10K20	6	144	24	24
EPF10K30 EPF10K30A	6	216	36	24
EPF10K40	8	216	36	24
EPF10K50 EPF10K50V	10	216	36	24
EPF10K70	9	312	52	24
EPF10K100 EPF10K100A	12	312	52	24
EPF10K130V	16	312	52	32
EPF10K250A	20	456	76	40

In addition to general-purpose I/O pins, FLEX 10K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device.

The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. However, the use of dedicated inputs as data inputs can introduce additional delay into the control signal network.

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Figure 12 shows the interconnection of adjacent LABs and EABs with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

Figure 12. Interconnect Resources
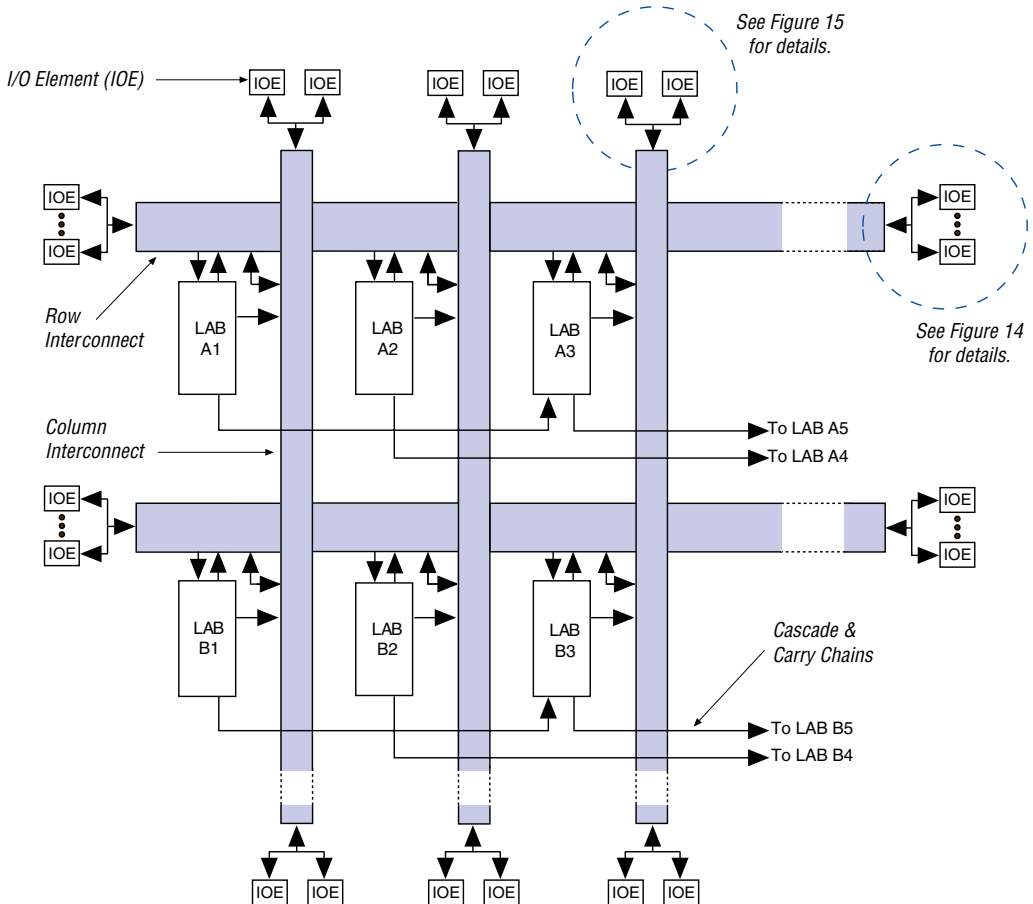
I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. The Quartus and MAX+PLUS II Compilers use the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Figure 13 shows the IOE block diagram.

Figure 13. Bidirectional I/O Registers
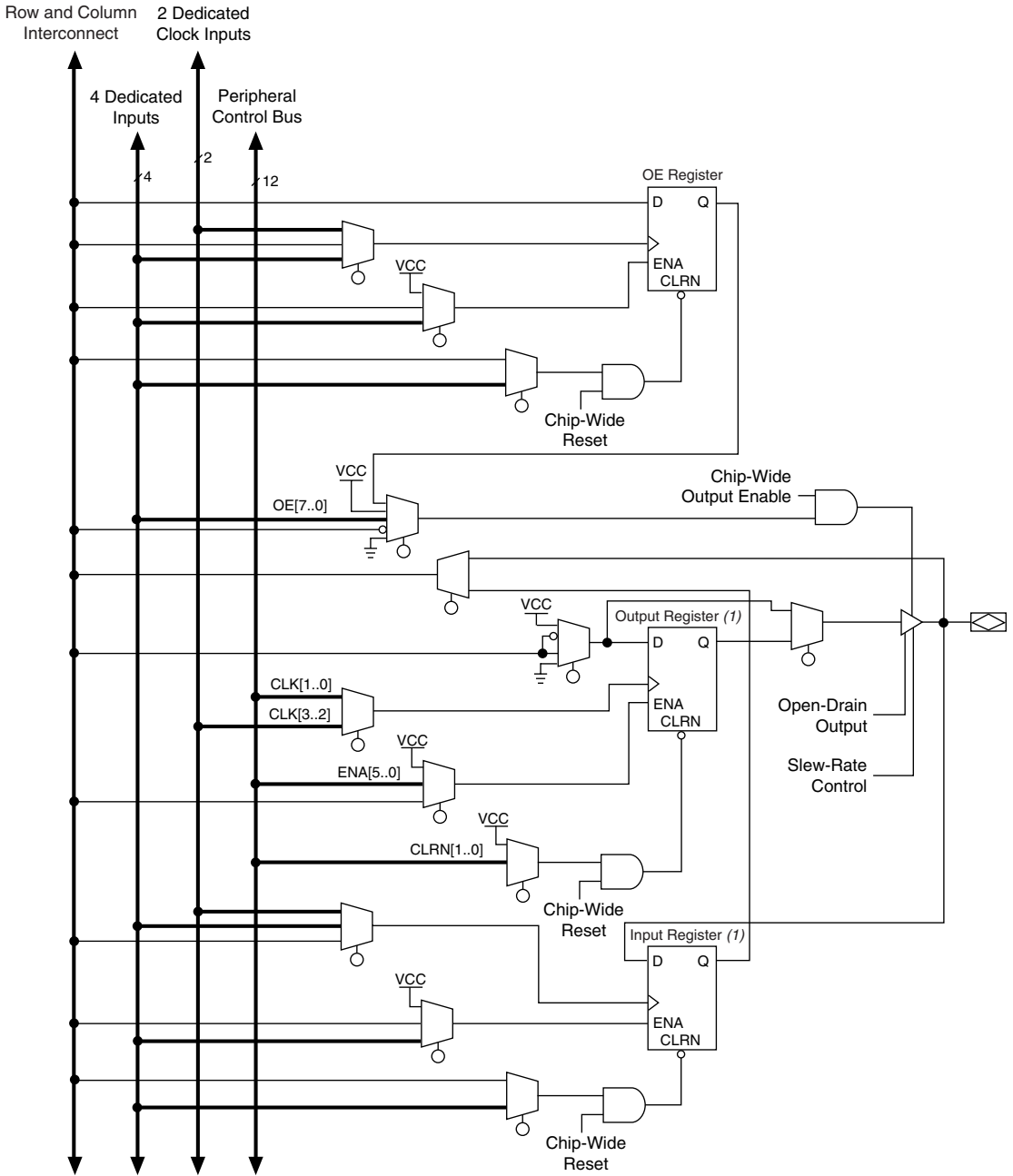
Row and Column
Interconnect

2 Dedicated
Clock Inputs

4 Dedicated
Inputs

Peripheral
Control Bus

OE Register

OE[7..0]

Chip-Wide
Reset

Chip-Wide
Output Enable

Output Register *(1)*

CLK[1..0]
CLK[3..2]

Open-Drain
Output

Slew-Rate
Control

ENA[5..0]

CLRN[1..0]

Chip-Wide
Reset

Input Register *(1)*

Chip-Wide
Reset

Note:
(1)   The output enable and input registers are LE registers in the lab adjacent to the
       bidirectional pin.

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Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal will reset all IOE registers, overriding any other control signals.

Tables 8 and 9 list the sources for each peripheral control signal, and the rows that can drive global signals. These tables also show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals.

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Table 8. EPF10K10, EPF10K20, EPF10K30, EPF10K40 & EPF10K50 Peripheral Bus Sources

Peripheral Control Signal	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
OE0	Row A	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C	Row B
OE2	Row B	Row C	Row C	Row D	Row D
OE3	Row B	Row D	Row D	Row E	Row F
OE4	Row C	Row E	Row E	Row F	Row H
OE5	Row C	Row F	Row F	Row G	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A	Row A	Row B	Row A
CLKENA1/OE6/GLOBAL1	Row A	Row B	Row B	Row C	Row C
CLKENA2/CLR0	Row B	Row C	Row C	Row D	Row E
CLKENA3/OE7/GLOBAL2	Row B	Row D	Row D	Row E	Row G
CLKENA4/CLR1	Row C	Row E	Row E	Row F	Row I
CLKENA5/CLK1/GLOBAL3	Row C	Row F	Row F	Row H	Row J

Table 9. EPF10K70, EPF10K100, EPF10K130V & EPF10K250A Peripheral Bus Sources

Peripheral Control Signal	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
OE0	Row A	Row A	Row C	Row E
OE1	Row B	Row C	Row E	Row G
OE2	Row D	Row E	Row G	Row I
OE3	Row I	Row L	Row N	Row P
OE4	Row G	Row I	Row K	Row M
OE5	Row H	Row K	Row M	Row O
CLKENA0/CLK0/GLOBAL0	Row E	Row F	Row H	Row J
CLKENA1/OE6/GLOBAL1	Row C	Row D	Row F	Row H
CLKENA2/CLR0	Row B	Row B	Row D	Row F
CLKENA3/OE7/GLOBAL2	Row F	Row H	Row J	Row L
CLKENA4/CLR1	Row H	Row J	Row L	Row N
CLKENA5/CLK1/GLOBAL3	Row E	Row G	Row I	Row K

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. The internally generated signal can drive the global signal, providing the same low-skew, low-delay characteristics for an internally generated signal as for a signal driven by an input. This feature is ideal for internally generated clear or clock signals with high fan-out. When a global signal is driven by internal logic, the dedicated input pin that drives that global signal cannot be used. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

When the chip-wide output enable pin is held low, it will tri-state all pins on the device. This option can be set in the Global Project Device Options menu. Additionally, the registers in the IOE can be reset by holding the chip-wide reset pin low.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel. See Figure 14.

Figure 14. FLEX 10K Row-to-IOE Connections

The values for m and n are provided in Table 10.

Each IOE is driven by an m-to-1 multiplexer.

Each IOE can drive up to two row channels.

Table 10 lists the FLEX 10K row-to-IOE interconnect resources.

Table 10. FLEX 10K Row-to-IOE Interconnect Resources		
Device	**Channels per Row (*n*)**	**Row Channels per Pin (*m*)**
EPF10K10 EPF10K10A	144	18
EPF10K20	144	18
EPF10K30 EPF10K30A	216	27
EPF10K40	216	27
EPF10K50 EPF10K50V	216	27
EPF10K70	312	39
EPF10K100 EPF10K100A	312	39
EPF10K130V	312	39
EPF10K250A	456	57

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels that each IOE can access is different for each IOE. See Figure 15.

Figure 15. FLEX 10K Column-to-IOE Connections

The values for m and n are provided in Table 11.
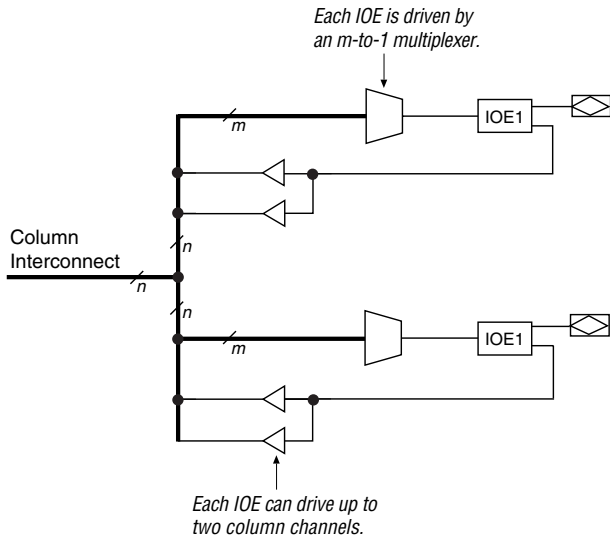
Table 11 lists the FLEX 10K column-to-IOE interconnect resources.

Table 11. FLEX 10K Column-to-IOE Interconnect Resources		
Device	**Channels per Column (n)**	**Column Channel per Pin (m)**
EPF10K10 EPF10K10A	24	16
EPF10K20	24	16
EPF10K30 EPF10K30A	24	16
EPF10K40	24	16
EPF10K50 EPF10K50V	24	16
EPF10K70	24	16
EPF10K100 EPF10K100A	24	16
EPF10K130V	32	24
EPF10K250A	40	32

SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Quartus and MAX+PLUS II software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The MAX+PLUS II software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 16).

Figure 16. SameFrame Pin-Out Example

Printed Circuit Board
Designed for 256-PinFineLine BGA Package

100-Pin FineLine BGA Package
(Reduced I/O Count or
Logic Requirements)

256-Pin FineLine BGA Package
(Increased I/O Count or
Logic Requirements)
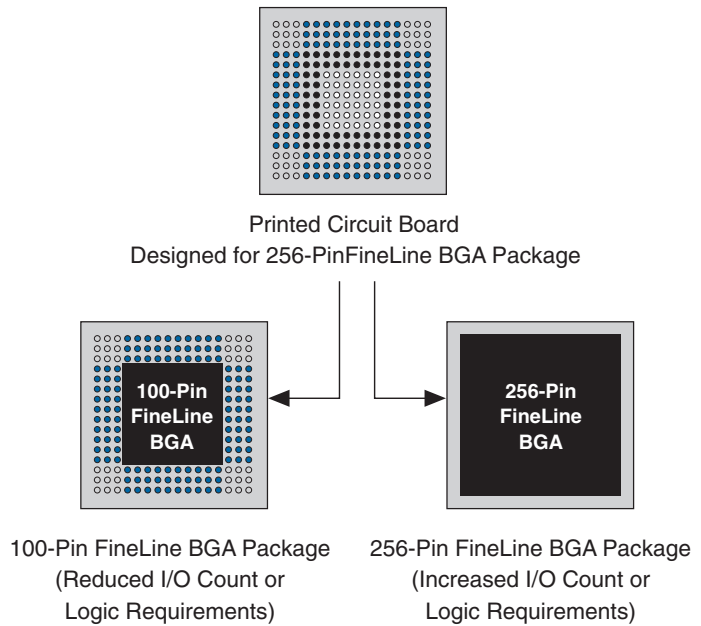
ClockLock & ClockBoost Features

To support high-speed designs, selected FLEX 10K devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in FLEX 10K devices are enabled through the MAX+PLUS II software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can only drive the clock inputs of registers; the generated clock cannot be gated or inverted.

The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

In designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to GCLK1. With the MAX+PLUS II software, GCLK1 can feed both the ClockLock and ClockBoost circuitry in the FLEX 10K device. However, when both circuits are used, the other clock pin (GCLK0) cannot be used. Figure 17 shows a block diagram of how to enable both the ClockLock and ClockBoost circuits in the MAX+PLUS II software. The example shown is a schematic, but a similar approach applies for designs created in AHDL, VHDL, and Verilog HDL. When the ClockLock and ClockBoost circuits are used simultaneously, the input frequency parameter must be the same for both circuits. In Figure 17, the input frequency must meet the requirements specified when the ClockBoost multiplication factor is two.

Figure 17. Enabling ClockLock & ClockBoost in the Same Design
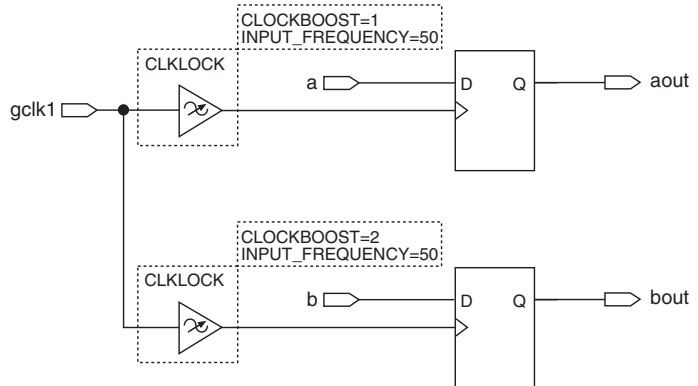
To use both the ClockLock and ClockBoost circuits in the same design, designers must use Revision C EPF10K100GC503-3DX devices and MAX+PLUS II software versions 7.2 or higher. The die revision is indicated by the third digit of the nine-digit code on the top side of the device.

For more information on using the ClockLock and ClockBoost features, see the *Clock Management with ClockLock & ClockBoost Features White Paper*, which is available from Altera Literature Services.

Output Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, MultiVolt I/O interface, and power sequencing for FLEX 10K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via MAX+PLUS II logic options. The MultiVolt I/O interface is controlled by connecting V_{CCIO} to a different voltage than V_{CCINT}. Its effect can be simulated in the MAX+PLUS II software via the **Global Project Device Options** dialog box (Assign menu).

PCI Clamping Diodes

The EPF10K10A and EPF10K30A devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the transient overshoot caused by reflected waves to the V_{CCIO} value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis via a logic option in the MAX+PLUS II software. When V_{CCIO} is 3.3 V, a pin that has the clamping diode turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When V_{CCIO} is 2.5 V, a pin that has the clamping diode turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. However, a clamping diode can be turned on for a subset of pins, which allows devices to bridge between a 3.3-V PCI bus and a 5.0-V device.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of approximately 2.9 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane. Additionally, the MAX+PLUS II software can convert tri-state buffers with grounded data inputs to open-drain pins automatically.

Open-drain output pins on FLEX 10K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 10K devices with V_{CCIO} = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

MultiVolt I/O Interface

The FLEX 10K device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10K devices to interface with systems of differing supply voltages. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT) and another set for I/O output drivers (VCCIO).

Table 12 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

Table 12. Supply Voltages & MultiVolt I/O Support Levels

Devices	Supply Voltage (V)		MultiVolt I/O Support Levels (V)	
	V_{CCINT}	V_{CCIO}	Input	Output
FLEX 10K *(1)*	5.0	5.0	3.3 or 5.0	5.0
	5.0	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K50V *(1)*	3.3	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K130V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
FLEX 10KA *(1)*	3.3	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	3.3	2.5	2.5, 3.3, or 5.0	2.5

Note
(1)   The 240 pin QFP pagckages do not support the MultiVolt I/O feature so there are no V_{CCIO} pins.

Power Sequencing & Hot-Socketing

Because FLEX 10K devices can be used in a multi-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into FLEX 10KA devices before and during power up without damaging the device. Additionally, FLEX 10KA devices do not drive out during power up. Once operating conditions are reached, FLEX 10KA devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, ByteBlaster parallel port download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 13.

Table 13. FLEX 10K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a FLEX 10K device via JTAG ports with a BitBlaster, ByteBlaster, or ByteBlasterMV download cable, or using a Jam File (**.jam**) or Jam Byte-Code File (**.jbc**) via an embedded processor.

The instruction register length of FLEX 10K devices is 10 bits. The USERCODE register length in FLEX 10K devices is 32 bits; 7 bits are determined by the user, and 25 bits are predetermined. Tables 14 and 15 show the boundary-scan register length and device IDCODE information for FLEX 10K devices.

Table 14. FLEX 10K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPF10K10, EPF10K10A	480
EPF10K20	624
EPF10K30, EPF10K30A	768
EPF10K40	864
EPF10K50, EPF10K50V	960
EPF10K70	1,104
EPF10K100, EPF10K100A	1,248
EPF10K130V	1,440
EPF10K250A	1,440

Table 15. 32-Bit FLEX 10K Device IDCODE   *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	**Part Number (16 Bits)**	**Manufacturer's Identity (11 Bits)**	**1 (1 Bit)** *(2)*
EPF10K10, EPF10K10A	0000	0001 0000 0001 0000	00001101110	1
EPF10K20	0000	0001 0000 0010 0000	00001101110	1
EPF10K30, EPF10K30A	0000	0001 0000 0011 0000	00001101110	1
EPF10K40	0000	0001 0000 0100 0000	00001101110	1
EPF10K50, EPF10K50V	0000	0001 0000 0101 0000	00001101110	1
EPF10K70	0000	0001 0000 0111 0000	00001101110	1
EPF10K100, EPF10K100A	0000	0000 0001 0000 0000	00001101110	1
EPF10K130V	0000	0000 0001 0011 0000	00001101110	1
EPF10K250A	0000	0000 0010 0101 0000	00001101110	1

Notes:
(1)   The most significant bit (MSB) is on the left.
(2)   The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10K devices include weak pull-ups on JTAG pins.

For more information, see the following documents:

- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlaster Parallel Port Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Figure 18 shows the timing requirements for the JTAG signals.

Figure 18. JTAG Waveforms
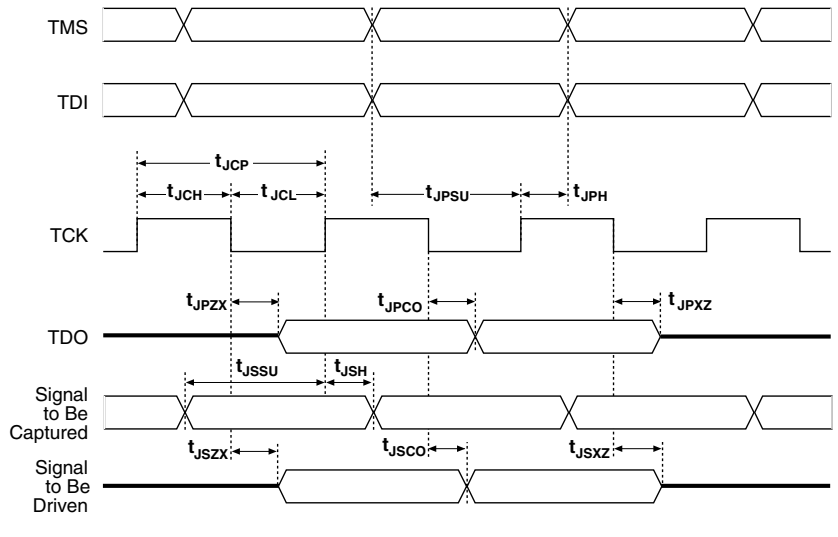
Table 16 shows the timing parameters and values for FLEX 10K devices.

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high-impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Table 16. JTAG Timing Parameters & Values

Generic Testing

Each FLEX 10K device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10K devices are made under conditions equivalent to those shown in Figure 19. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 19. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.

VCC

464 Ω
(703 Ω)
[521 Ω]

Device Output

To Test System

250 Ω
(8.06 kΩ)
[481 Ω]

C1 (includes JIG capacitance)

Device input rise and fall times < 3 ns
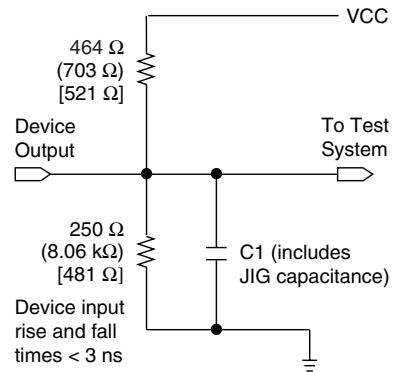
Operating Conditions

Tables 17 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 5.0-V FLEX 10K devices.

Table 17. FLEX 10K 5.0-V Device Absolute Maximum Ratings   *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	−2.0	7.0	V
V_I	DC input voltage		−2.0	7.0	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP, TQFP, RQFP, and BGA packages, under bias		135	° C

Table 18. FLEX 10K 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		−0.5	$V_{CCINT} + 0.5$	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 19. FLEX 10K 5.0-V Device DC Operating Conditions   *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CCINT} + 0.5$	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 4.75$ V *(7)*	2.4			V
	3.3-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 3.00$ V *(7)*	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V *(7)*	$V_{CCIO} - 0.2$			V
V_{OL}	5.0-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 4.75$ V *(8)*			0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V *(8)*			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V *(8)*			0.2	V
I_I	Input pin leakage current	$V_I = V_{CC}$ or ground	−10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CC}$ or ground	−40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	10	mA

Table 20. 5.0-V Device Capacitance of EPF10K10, EPF10K20 & EPF10K30 Devices *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Table 21. 5.0-V Device Capacitance of EPF10K40, EPF10K50, EPF10K70 & EPF10K100 Devices *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:
(1)   See the *Operating Requirements for Altera Devices Data Sheet*.
(2)   Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3)   Numbers in parentheses are for industrial-temperature-range devices.
(4)   Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5)   Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6)   These values are specified under Table 18 on page 44.
(7)   The I_{OH} parameter refers to high-level TTL or CMOS output current.
(8)   The I_{OL} parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9)   Capacitance is sample-tested only.

Figure 20 shows the typical output drive characteristics of FLEX 10K devices with 5.0-V and 3.3-V V_{CCIO}. The output driver is compliant with the 5.0-V *PCI Local Bus Specification, Revision 2.2* (for 5.0-V V_{CCIO}).

Figure 20. Output Drive Characteristics of FLEX 10K Devices
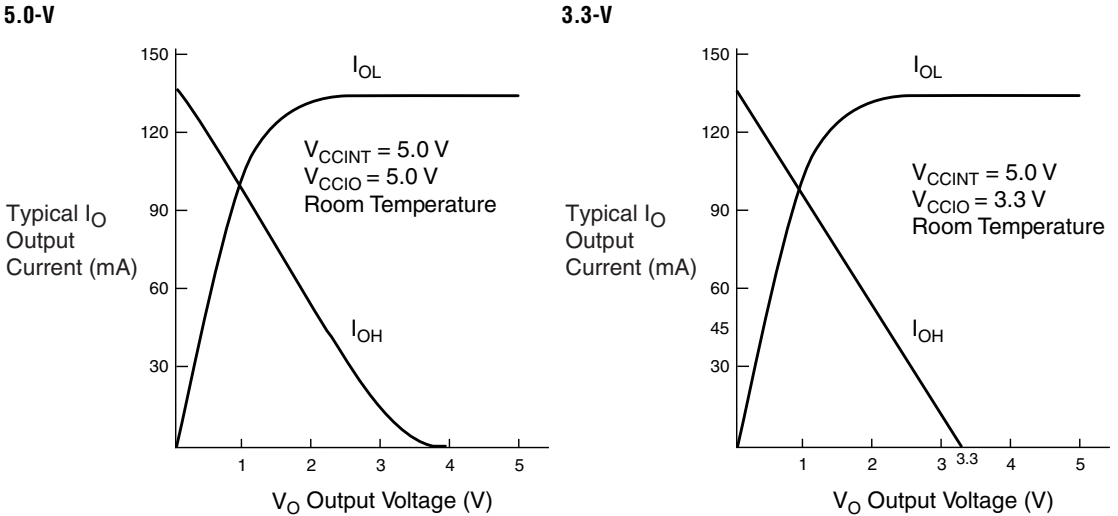
Tables 22 through 25 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for EPF10K50V and EPF10K130V devices.

Table 22. EPF10K50V & EPF10K130V Device Absolute Maximum Ratings			*Note (1)*		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	With respect to ground *(2)*	–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		RQFP and BGA packages, under bias		135	° C

Table 23. EPF10K50V & EPF10K130V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage	*(5)*	-0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 24. EPF10K50V & EPF10K130V Device DC Operating Conditions   *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		5.75	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC *(8)*	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC *(8)*	$V_{CCIO} - 0.2$			V
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC *(9)*			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC *(9)*			0.2	V
I_I	Input pin leakage current	$V_I = 5.3$ V to −0.3 V	−10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = 5.3$ V to −0.3 V	−10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.3	10	mA
		V_I = ground, no load *(10)*		10		mA

Table 25. EPF10K50V & EPF10K130V Device Capacitance   *Note (11)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:
(1)   See the *Operating Requirements for Altera Devices Data Sheet*.
(2)   Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3)   Numbers in parentheses are for industrial-temperature-range devices.
(4)   Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5)   EPF10K50V and EPF10K130V device inputs may be driven before V_{CCINT} and V_{CCIO} are powered.
(6)   Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7)   These values are specified under the EPF10K50V and EPF10K130V device recommended operating conditions in Table 23 on page 47.
(8)   The I_{OH} parameter refers to high-level TTL or CMOS output current.
(9)   The I_{OL} parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10)   This parameter applies to -1 speed grade EPF10K50V devices, -2 speed grade EPF10K50V industrial temperature devices, and -2 speed grade EPF10K130V devices.
(11)   Capacitance is sample-tested only.

Figure 21 shows the typical output drive characteristics of EPF10K50V and EPF10K130V devices.

Figure 21. Output Drive Characteristics of EPF10K50V & EPF10K130V Devices
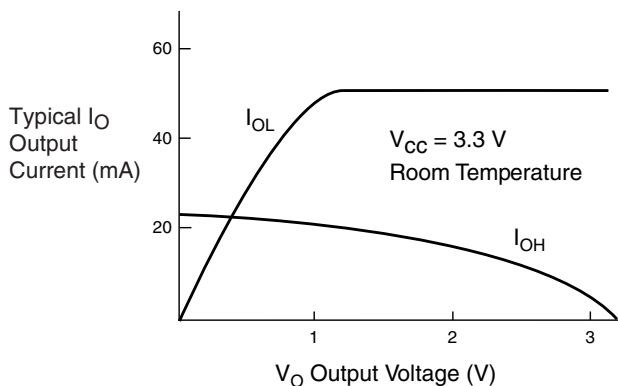
Tables 26 through 31 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 3.3-V FLEX 10K devices.

Table 26. FLEX 10KA 3.3-V Device Absolute Maximum Ratings   *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	−0.5	4.6	V
V_I	DC input voltage		−2.0	5.75	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP, TQFP, RQFP, and BGA packages, under bias		135	° C

Table 27. FLEX 10KA 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3), (4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3), (4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3), (4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*(5)*	−0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 28. FLEX 10KA 3.3-V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7 or $0.5 \times V_{CCINT}$, whichever is lower		5.75	V
V_{IL}	Low-level input voltage		−0.5		$0.3 \times V_{CCINT}$	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = −11 mA DC, V_{CCIO} = 3.00 V *(8)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = −0.1 mA DC, V_{CCIO} = 3.00 V *(8)*	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	I_{OH} = −0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(8)*	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	I_{OH} = −0.1 mA DC, V_{CCIO} = 2.30 V *(8)*	2.1			V
		I_{OH} = −1 mA DC, V_{CCIO} = 2.30 V *(8)*	2.0			V
		I_{OH} = −2 mA DC, V_{CCIO} = 2.30 V *(8)*	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 9 mA DC, V_{CCIO} = 3.00 V *(9)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(9)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(9)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(9)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(9)*			0.7	V
I_I	Input pin leakage current	V_I = 5.3 V to −0.3 V	−10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.3 V to −0.3 V	−10		10	μA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.3	10	mA
		V_I = ground, no load *(10)*		10		mA

Table 29. 3.3-V Device Capacitance of EPF10K10A & EPF10K30A Devices *Note (11)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Table 30. 3.3-V Device Capacitance of EPF10K100A Devices *Note (11)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Table 31. 3.3-V Device Capacitance of EPF10K250A Devices *Note (11)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:
(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC voltage input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns. FLEX 10KA devices can withstand a 11 V pulse for 11ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) FLEX 10KA device inputs may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) These values are specified under Table 27 on page 49.
(8) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(9) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10) This parameter applies to all -1 speed grade commercial temperature devices and all -2 speed grade industrial-temperature devices.
(11) Capacitance is sample-tested only.

Figure 22 shows the typical output drive characteristics of EPF10K10A, EPF10K30A, EPF10K100A, and EPF10K250A devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compliant with the 3.3-V *PCI Local Bus Specification*, *Revision 2.2* (with 3.3-V V_{CCIO}). Moreover, device analysis shows that the EPF10K10A, EPF10K30A, and EPF 10K100A devices can drive a 5.0-V PCI bus with eight or fewer loads.

Figure 22. Output Drive Characteristics for EPF10K10A, EPF10K30A & EPF10K100A Devices
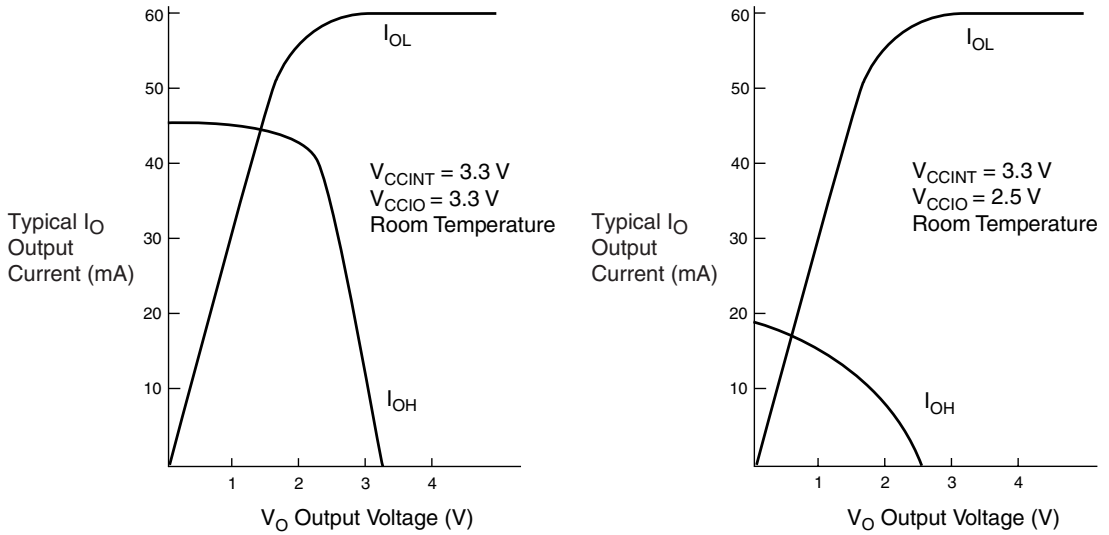
Figure 23 shows the typical output drive characteristics of the EPF10K250A device with 3.3-V and 2.5-V V_{CCIO}.

Figure 23. Output Drive Characteristics for EPF10K250A Device
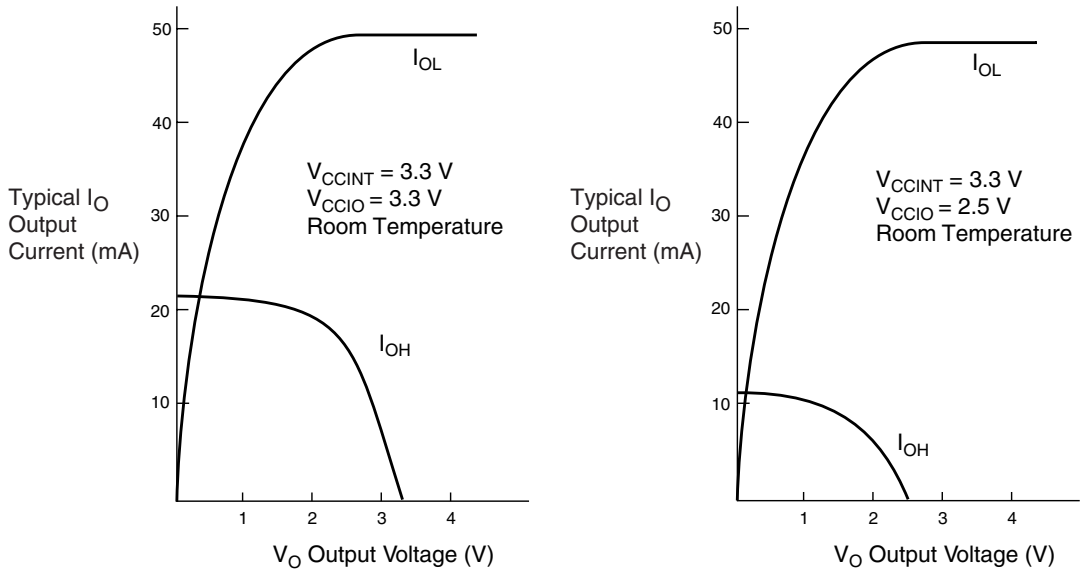
Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay (t_{CO})
- Interconnect delay ($t_{SAMEROW}$)
- LE look-up table delay (t_{LUT})
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10K device.

Figure 24. FLEX 10K Device Timing Model
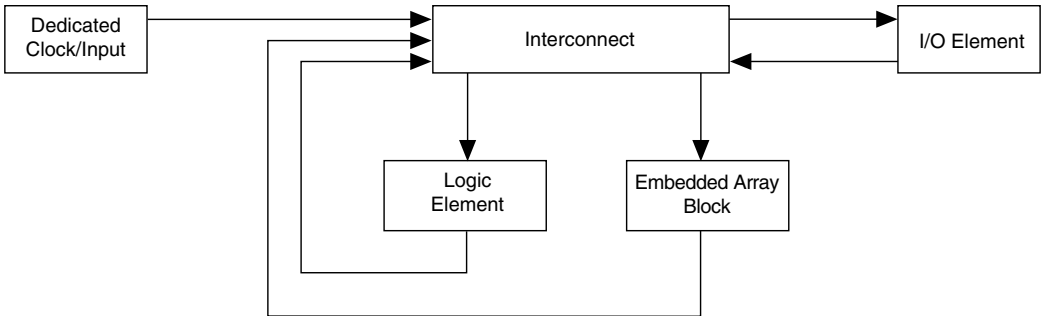
Figures 25 through 27 show the delays that correspond to various paths and functions within the LE, IOE, and EAB timing models.

Figure 25. FLEX 10K Device LE Timing Model
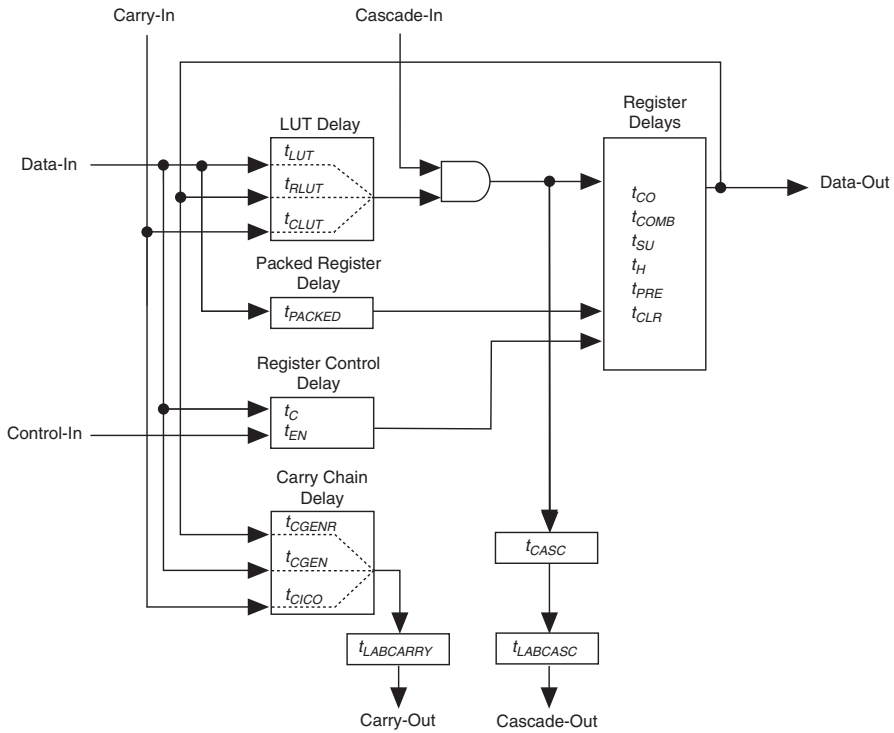
Figure 26. FLEX 10K Device IOE Timing Model
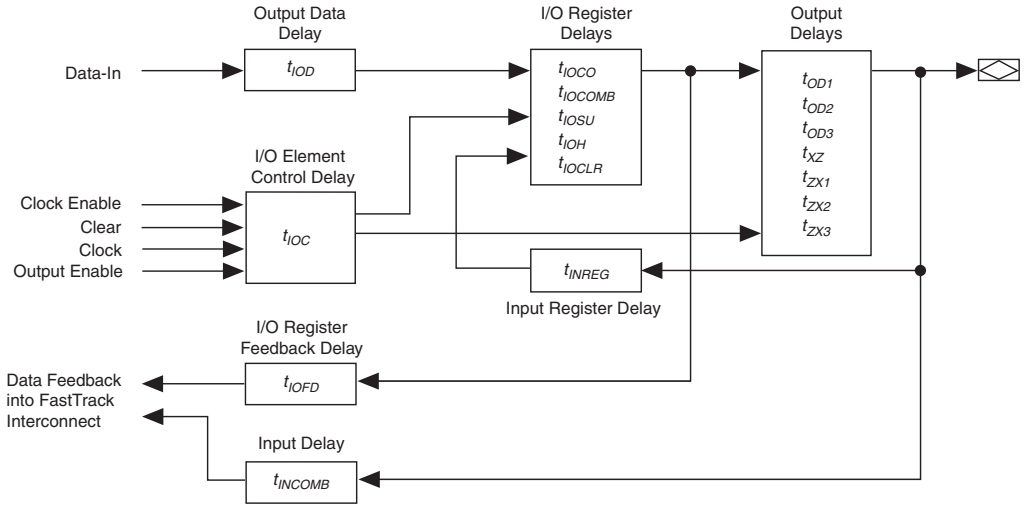
Figure 27. FLEX 10K Device EAB Timing Model
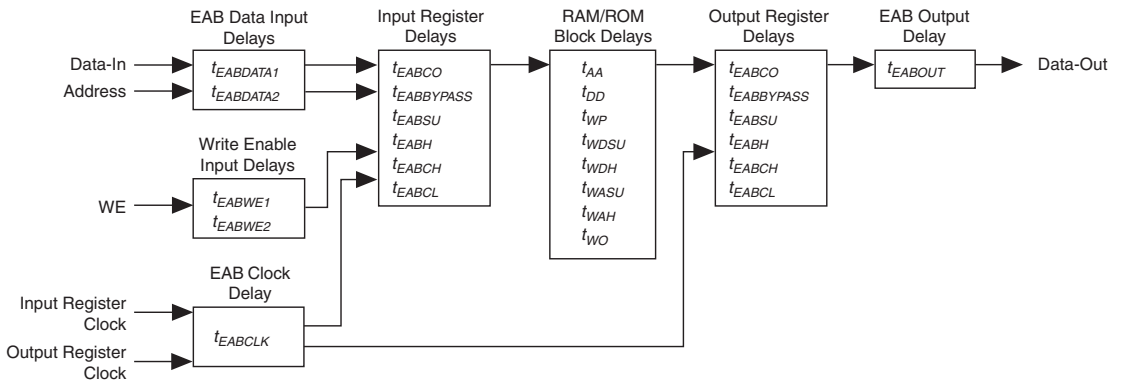
Figures 28 shows the timing model for bidirectional I/O pin timing.

Figure 28. Synchronous Bidirectional Pin External Timing Model
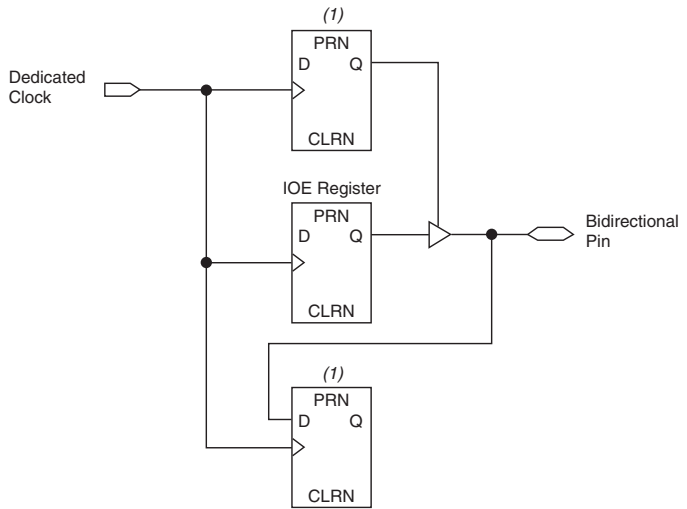
Note:
(1)   The output enable and input registers are LE registers in the lab adjacent to the bidirectional pin.

Tables 32 through 36 describe the FLEX 10K device internal timing parameters. These internal timing parameters are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and analysis. Tables 37 through 39 describe FLEX 10K external timing parameters.

Table 32. LE Timing Microparameters (Part 1 of 2)   *Note (1)*

Symbol	Parameter	Conditions
t_{LUT}	LUT delay for data-in	
t_{CLUT}	LUT delay for carry-in	
t_{RLUT}	LUT delay for LE register feedback	
t_{PACKED}	Data-in to packed register delay	
t_{EN}	LE register enable delay	
t_{CICO}	Carry-in to carry-out delay	
t_{CGEN}	Data-in to carry-out delay	
t_{CGENR}	LE register feedback to carry-out delay	
t_{CASC}	Cascade-in to cascade-out delay	
t_C	LE register control signal delay	

Table 32. LE Timing Microparameters (Part 2 of 2)   Note (1)

Symbol	Parameter	Conditions
t_{CO}	LE register clock-to-output delay	
t_{COMB}	Combinatorial delay	
t_{SU}	LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load	
t_H	LE register hold time for data and enable signals after clock	
t_{PRE}	LE register preset delay	
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

Table 33. IOE Timing Microparameters   Note (1)

Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register hold time for data and enable signals after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF (3)
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF (3)
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 34. EAB Timing Microparameters   *Note (1)*

Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABBYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	
t_{AA}	Address access delay	
t_{WP}	Write pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	*(5)*
t_{WDH}	Data hold time after falling edge of write pulse	*(5)*
t_{WASU}	Address setup time before rising edge of write pulse	*(5)*
t_{WAH}	Address hold time after falling edge of write pulse	*(5)*
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	

Table 35. EAB Timing Macroparameters   *Notes (1), (6)*

Symbol	Parameter	Conditions
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
$t_{EABWESH}$	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Table 36. Interconnect Timing Microparameters   *Note (1)*

Symbol	Parameter	Conditions
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*(7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*(7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*(7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*(7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*(7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*(7)*
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	*(7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*(7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	*(7)*
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	*(7)*

Table 37. External Reference Timing Parameters   *Note (8)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	*(9)*

Table 38. External Timing Parameters   *Note (10)*

Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	

Table 39. External Bidirectional Timing Parameters   *Note (10)*

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at adjacent LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at adjacent LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	

Notes to tables:
(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: V_{CCIO} = 5.0 V ± 5% for commercial use in FLEX 10K devices.
             V_{CCIO} = 5.0 V ± 10% for industrial use in FLEX 10K devices.
             V_{CCIO} = 3.3 V ± 10% for commercial or industrial use in FLEX 10KA devices.
(3) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial or industrial use in FLEX 10K devices.
             V_{CCIO} = 2.5 V ± 0.2 V for commercial or industrial use in FLEX 10KA devices.
(4) Operating conditions: V_{CCIO} = 2.5 V, 3.3 V, or 5.0 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(9) Contact Altera Applications for test circuit specifications and test conditions.
(10) These timing parameters are sample-tested only.

Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 34.

Figure 29. EAB Asynchronous Timing Waveforms

EAB Asynchronous Read
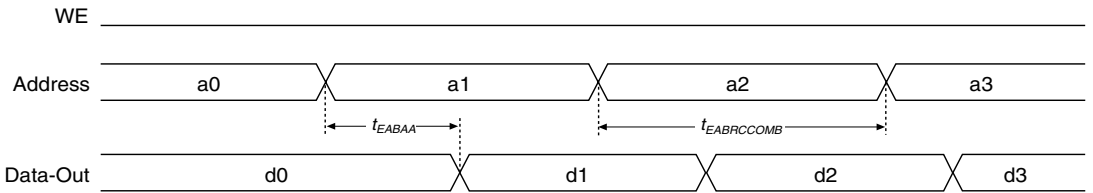
EAB Asynchronous Write
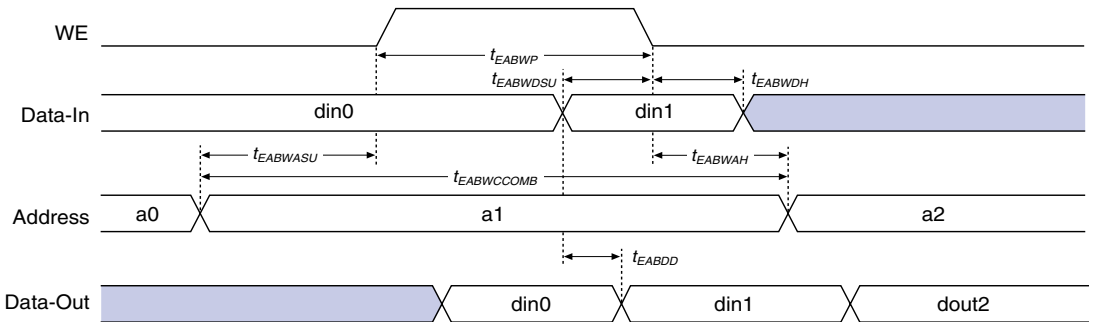
Figure 30. EAB Synchronous Timing Waveforms

EAB Synchronous Read
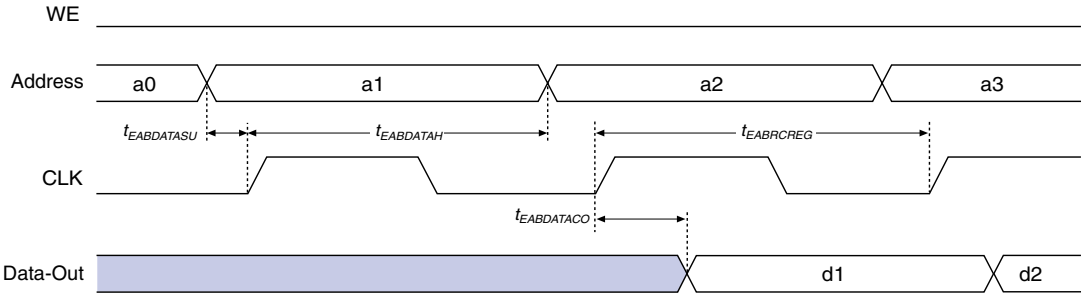
EAB Synchronous Write (EAB Output Registers Used)
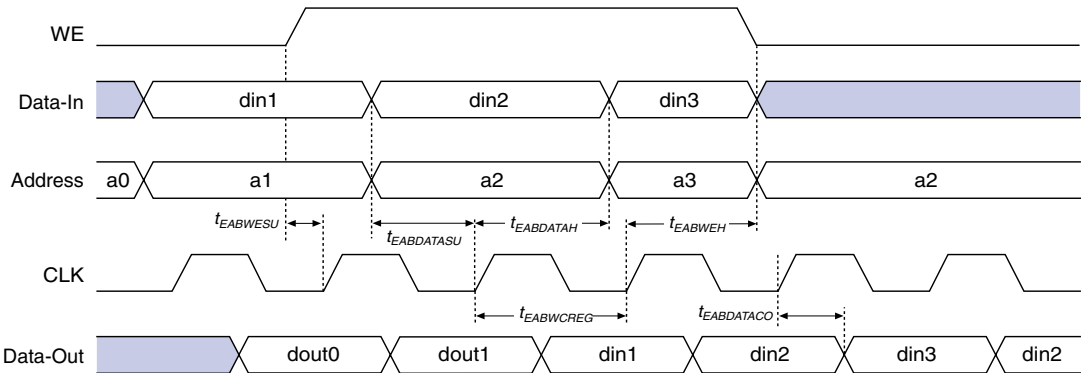
Tables 40 through 48 show EPF10K10 and EPF10K20 device internal and external timing parameters.

Table 40. EPF10K10 & EPF10K20 Device LE Timing Microparameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
t_{LUT}		1.4		1.7	ns
t_{CLUT}		0.6		0.7	ns
t_{RLUT}		1.5		1.9	ns
t_{PACKED}		0.6		0.9	ns
t_{EN}		1.0		1.2	ns
t_{CICO}		0.2		0.3	ns
t_{CGEN}		0.9		1.2	ns
t_{CGENR}		0.9		1.2	ns
t_{CASC}		0.8		0.9	ns
t_C		1.3		1.5	ns
t_{CO}		0.9		1.1	ns
t_{COMB}		0.5		0.6	ns
t_{SU}	1.3		2.5		ns
t_H	1.4		1.6		ns
t_{PRE}		1.0		1.2	ns
t_{CLR}		1.0		1.2	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Table 41. EPF10K10 & EPF10K20 Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
t_{IOD}		1.3		1.6	ns
t_{IOC}		0.5		0.7	ns
t_{IOCO}		0.2		0.2	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	2.8		3.2		ns
t_{IOH}	1.0		1.2		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		2.6		3.5	ns
t_{OD2}		4.9		6.4	ns
t_{OD3}		6.3		8.2	ns
t_{XZ}		4.5		5.4	ns
t_{ZX1}		4.5		5.4	ns
t_{ZX2}		6.8		8.3	ns
t_{ZX3}		8.2		10.1	ns
t_{INREG}		6.0		7.5	ns
t_{IOFD}		3.1		3.5	ns
t_{INCOMB}		3.1		3.5	ns

Table 42. EPF10K10 & EPF10K20 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.9	ns
$t_{EABDATA2}$		4.8		6.0	ns
t_{EABWE1}		1.0		1.2	ns
t_{EABWE2}		5.0		6.2	ns
t_{EABCLK}		1.0		2.2	ns
t_{EABCO}		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.9	ns
t_{EABSU}	1.5		1.8		ns
t_{EABH}	2.0		2.5		ns
t_{AA}		8.7		10.7	ns
t_{WP}	5.8		7.2		ns
t_{WDSU}	1.6		2.0		ns
t_{WDH}	0.3		0.4		ns
t_{WASU}	0.5		0.6		ns
t_{WAH}	1.0		1.2		ns
t_{WO}		5.0		6.2	ns
t_{DD}		5.0		6.2	ns
t_{EABOUT}		0.5		0.6	ns
t_{EABCH}	4.0		4.0		ns
t_{EABCL}	5.8		7.2		ns

Table 43. EPF10K10 & EPF10K20 Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	**Max**	**Min**	**Max**	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATACO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Table 44. EPF10K10 Device Interconnect Timing Microparameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.8		6.2	ns
t_{DIN2LE}		2.6		3.8	ns
$t_{DIN2DATA}$		4.3		5.2	ns
$t_{DCLK2IOE}$		3.4		4.0	ns
$t_{DCLK2LE}$		2.6		3.8	ns
$t_{SAMELAB}$		0.6		0.6	ns
$t_{SAMEROW}$		3.6		3.8	ns
$t_{SAMECOLUMN}$		0.9		1.1	ns
$t_{DIFFROW}$		4.5		4.9	ns
$t_{TWOROWS}$		8.1		8.7	ns
$t_{LEPERIPH}$		3.3		3.9	ns
$t_{LABCARRY}$		0.5		0.8	ns
$t_{LABCASC}$		2.7		3.0	ns

Table 45. EPF10K20 Device Interconnect Timing Microparameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
$t_{DIN2IOE}$		5.2		6.6	ns
t_{DIN2LE}		2.6		3.8	ns
$t_{DIN2DATA}$		4.3		5.2	ns
$t_{DCLK2IOE}$		4.3		4.0	ns
$t_{DCLK2LE}$		2.6		3.8	ns
$t_{SAMELAB}$		0.6		0.6	ns
$t_{SAMEROW}$		3.7		3.9	ns
$t_{SAMECOLUMN}$		1.4		1.6	ns
$t_{DIFFROW}$		5.1		5.5	ns
$t_{TWOROWS}$		8.8		9.4	ns
$t_{LEPERIPH}$		4.7		5.6	ns
$t_{LABCARRY}$		0.5		0.8	ns
$t_{LABCASC}$		2.7		3.0	ns

Table 46. EPF10K10 & EPF10K20 Device External Timing Parameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		**-4**		
	Min	**Max**	**Min**	**Max**	
t_{DRR}		16.1		20.0	ns
t_{INSU} *(2), (3)*	5.5		6.0		ns
t_{INH} *(3)*	0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	6.7	2.0	8.4	ns

Table 47. EPF10K10 Device External Bidirectional Timing Parameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		**-4**		
	Min	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$	4.5		5.6		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.7	2.0	8.4	ns
$t_{XZBIDIR}$		10.5		13.4	ns
$t_{ZXBIDIR}$		10.5		13.4	ns

Table 48. EPF10K20 Device External Bidirectional Timing Parameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		**-4**		
	Min	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$	4.6		5.7		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.7	2.0	8.4	ns
$t_{XZBIDIR}$		10.5		13.4	ns
$t_{ZXBIDIR}$		10.5		13.4	ns

Notes to tables:
(1)   All timing parameters are described in Tables 32 through 39 in this data sheet.
(2)   Using an LE to register the signal may provide a lower setup time.
(3)   This parameter is specified by characterization.

Tables 49 through 57 show EPF10K30, EPF10K40, and EPF10K50 device internal and external timing parameters.

Symbol	Speed Grade				Unit
	-3		**-4**		
	Min	Max	Min	Max	
t_{LUT}		1.3		1.8	ns
t_{CLUT}		0.6		0.6	ns
t_{RLUT}		1.5		2.0	ns
t_{PACKED}		0.5		0.8	ns
t_{EN}		0.9		1.5	ns
t_{CICO}		0.2		0.4	ns
t_{CGEN}		0.9		1.4	ns
t_{CGENR}		0.9		1.4	ns
t_{CASC}		1.0		1.2	ns
t_C		1.3		1.6	ns
t_{CO}		0.9		1.2	ns
t_{COMB}		0.6		0.6	ns
t_{SU}	1.4		1.4		ns
t_H	0.9		1.3		ns
t_{PRE}		0.9		1.2	ns
t_{CLR}		0.9		1.2	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Table 49. EPF10K30, EPF10K40 & EPF10K50 Device LE Timing Microparameters *Note (1)*

Table 50. EPF10K30, EPF10K40 & EPF10K50 Device IOE Timing Microparameters *Note (1)*					
Symbol	**Speed Grade**				**Unit**
	-3		**-4**		
	Min	**Max**	**Min**	**Max**	
t_{IOD}		0.4		0.6	ns
t_{IOC}		0.5		0.9	ns
t_{IOCO}		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	3.1		3.5		ns
t_{IOH}	1.0		1.9		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		3.3		3.6	ns
t_{OD2}		5.6		6.5	ns
t_{OD3}		7.0		8.3	ns
t_{XZ}		5.2		5.5	ns
t_{ZX1}		5.2		5.5	ns
t_{ZX2}		7.5		8.4	ns
t_{ZX3}		8.9		10.2	ns
t_{INREG}		7.7		10.0	ns
t_{IOFD}		3.3		4.0	ns
t_{INCOMB}		3.3		4.0	ns

Table 51. EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Microparameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.9	ns
$t_{EABDATA2}$		4.8		6.0	ns
t_{EABWE1}		1.0		1.2	ns
t_{EABWE2}		5.0		6.2	ns
t_{EABCLK}		1.0		2.2	ns
t_{EABCO}		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.9	ns
t_{EABSU}	1.5		1.8		ns
t_{EABH}	2.0		2.5		ns
t_{AA}		8.7		10.7	ns
t_{WP}	5.8		7.2		ns
t_{WDSU}	1.6		2.0		ns
t_{WDH}	0.3		0.4		ns
t_{WASU}	0.5		0.6		ns
t_{WAH}	1.0		1.2		ns
t_{WO}		5.0		6.2	ns
t_{DD}		5.0		6.2	ns
t_{EABOUT}		0.5		0.6	ns
t_{EABCH}	4.0		4.0		ns
t_{EABCL}	5.8		7.2		ns

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Table 52. EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Timing Macroparameters					*Note (1)*
Symbol	**Speed Grade**				**Unit**
	-3		**-4**		
	Min	**Max**	**Min**	**Max**	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATACO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Table 53. EPF10K30 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
$t_{DIN2IOE}$		6.9		8.7	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		2.5		2.7	ns
$t_{DIFFROW}$		5.8		6.4	ns
$t_{TWOROWS}$		9.1		10.1	ns
$t_{LEPERIPH}$		6.2		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Table 54. EPF10K40 Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.6		9.4	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		3.1		3.2	ns
$t_{DIFFROW}$		6.4		6.4	ns
$t_{TWOROWS}$		9.7		10.6	ns
$t_{LEPERIPH}$		6.4		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Table 55. EPF10K50 Device Interconnect Timing Microparameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
$t_{DIN2IOE}$		8.4		10.2	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		3.9		4.1	ns
$t_{DIFFROW}$		7.2		7.8	ns
$t_{TWOROWS}$		10.5		11.5	ns
$t_{LEPERIPH}$		7.5		8.2	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Table 56. EPF10K30, EPF10K40 & EPF10K50 Device External Timing Parameters   *Note (1)*

Symbol	Speed Grade				Unit
	-3		-4		
	Min	Max	Min	Max	
t_{DRR}		17.2		21.1	ns
t_{INSU} (2), (3)	5.7		6.4		ns
t_{INH} (3)	0.0		0.0		ns
t_{OUTCO} (3)	2.0	8.8	2.0	11.2	ns

Table 57. EPF10K30, EPF10K40 & EPF10K50 Device External Bidirectional Timing Parameters *(1)*

Symbol	Speed Grade				Unit
	-3		**-4**		
	Min	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$	4.1		4.6		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	8.8	2.0	11.2	ns
$t_{XZBIDIR}$		12.3		15.0	ns
$t_{ZXBIDIR}$		12.3		15.0	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 39 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 58 through 64 show EPF10K70 device internal and external timing parameters.

Table 58. EPF10K70 Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		1.3		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.5		1.6		2.0	ns
t_{PACKED}		0.8		0.9		1.3	ns
t_{EN}		0.8		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.0		1.1		1.4	ns
t_{CGENR}		1.1		1.2		1.5	ns
t_{CASC}		1.0		1.1		1.3	ns
t_C		0.7		0.8		1.0	ns
t_{CO}		0.9		1.0		1.4	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	1.9		2.1		2.6		ns
t_H	2.1		2.3		3.1		ns
t_{PRE}		0.9		1.0		1.4	ns
t_{CLR}		0.9		1.0		1.4	ns

Table 58. EPF10K70 Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 59. EPF10K70 Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		0.0		0.0		0.0	ns
t_{IOC}		0.4		0.5		0.7	ns
t_{IOCO}		0.4		0.4		0.9	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	4.5		5.0		6.2		ns
t_{IOH}	0.4		0.5		0.7		ns
t_{IOCLR}		0.6		0.7		1.6	ns
t_{OD1}		3.6		4.0		5.0	ns
t_{OD2}		5.6		6.3		7.3	ns
t_{OD3}		6.9		7.7		8.7	ns
t_{XZ}		5.5		6.2		6.8	ns
t_{ZX1}		5.5		6.2		6.8	ns
t_{ZX2}		7.5		8.5		9.1	ns
t_{ZX3}		8.8		9.9		10.5	ns
t_{INREG}		8.0		9.0		10.2	ns
t_{IOFD}		7.2		8.1		10.3	ns
t_{INCOMB}		7.2		8.1		10.3	ns

Table 60. EPF10K70 Device EAB Internal Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.3		1.5		1.9	ns
$t_{EABDATA2}$		4.3		4.8		6.0	ns
t_{EABWE1}		0.9		1.0		1.2	ns
t_{EABWE2}		4.5		5.0		6.2	ns
t_{EABCLK}		0.9		1.0		2.2	ns
t_{EABCO}		0.4		0.5		0.6	ns
$t_{EABBYPASS}$		1.3		1.5		1.9	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	1.8		2.0		2.5		ns
t_{AA}		7.8		8.7		10.7	ns
t_{WP}	5.2		5.8		7.2		ns
t_{WDSU}	1.4		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.4		0.5		0.6		ns
t_{WAH}	0.9		1.0		1.2		ns
t_{WO}		4.5		5.0		6.2	ns
t_{DD}		4.5		5.0		6.2	ns
t_{EABOUT}		0.4		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.2		5.8		7.2		ns

Table 61. EPF10K70 Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		-3		-4		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		12.1		13.7		17.0	ns
$t_{EABRCCOMB}$	12.1		13.7		17.0		ns
$t_{EABRCREG}$	8.6		9.7		11.9		ns
t_{EABWP}	5.2		5.8		7.2		ns
$t_{EABWCCOMB}$	6.5		7.3		9.0		ns
$t_{EABWCREG}$	11.6		13.0		16.0		ns
t_{EABDD}		8.8		10.0		12.5	ns
$t_{EABDATACO}$		1.7		2.0		3.4	ns
$t_{EABDATASU}$	4.7		5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.9		5.5		5.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.8		2.1		2.7		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	4.1		4.7		5.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		8.4		9.5		11.8	ns

Table 62. EPF10K70 Device Interconnect Timing Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.6		7.3		8.8	ns
t_{DIN2LE}		4.2		4.8		6.0	ns
$t_{DIN2DATA}$		6.5		7.1		10.8	ns
$t_{DCLK2IOE}$		5.5		6.2		7.7	ns
$t_{DCLK2LE}$		4.2		4.8		6.0	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.8		4.9		5.5	ns
$t_{SAMECOLUMN}$		3.3		3.4		3.7	ns
$t_{DIFFROW}$		8.1		8.3		9.2	ns
$t_{TWOROWS}$		12.9		13.2		14.7	ns
$t_{LEPERIPH}$		5.5		5.7		6.5	ns
$t_{LABCARRY}$		0.8		0.9		1.1	ns
$t_{LABCASC}$		2.7		3.0		3.2	ns

Table 63. EPF10K70 Device External Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		17.2		19.1		24.2	ns
t_{INSU} *(2), (3)*	6.6		7.3		8.0		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	9.9	2.0	11.1	2.0	14.3	ns

Table 64. EPF10K70 Device External Bidirectional Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$	7.4		8.1		10.4		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	9.9	2.0	11.1	2.0	14.3	ns
$t_{XZBIDIR}$		13.7		15.4		18.5	ns
$t_{ZXBIDIR}$		13.7		15.4		18.5	ns

Notes to tables:
(1)   All timing parameters are described in Tables 32 through 39 in this data sheet.
(2)   Using an LE to register the signal may provide a lower setup time.
(3)   This parameter is specified by characterization.

Tables 65 through 71 show EPF10K100 device internal and external timing parameters.

Table 65. EPF10K100 Device LE Timing Microparameters (Part 1 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-3DX		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		1.5		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.6		1.6		2.0	ns
t_{PACKED}		0.9		0.9		1.3	ns
t_{EN}		0.9		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.1		1.1		1.4	ns
t_{CGENR}		1.2		1.2		1.5	ns
t_{CASC}		1.1		1.1		1.3	ns
t_{C}		0.8		0.8		1.0	ns
t_{CO}		1.0		1.0		1.4	ns
t_{COMB}		0.5		0.5		0.7	ns
t_{SU}	2.1		2.1		2.6		ns
t_{H}	2.3		2.3		3.1		ns
t_{PRE}		1.0		1.0		1.4	ns
t_{CLR}		1.0		1.0		1.4	ns

Table 65. EPF10K100 Device LE Timing Microparameters (Part 2 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-3DX		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 66. EPF10K100 Device IOE Timing Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-3DX		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		0.0		0.0		0.0	ns
t_{IOC}		0.5		0.5		0.7	ns
t_{IOCO}		0.4		0.4		0.9	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	5.5		5.5		6.7		ns
t_{IOH}	0.5		0.5		0.7		ns
t_{IOCLR}		0.7		0.7		1.6	ns
t_{OD1}		4.0		4.0		5.0	ns
t_{OD2}		6.3		6.3		7.3	ns
t_{OD3}		7.7		7.7		8.7	ns
t_{XZ}		6.2		6.2		6.8	ns
t_{ZX1}		6.2		6.2		6.8	ns
t_{ZX2}		8.5		8.5		9.1	ns
t_{ZX3}		9.9		9.9		10.5	ns
t_{INREG} without ClockLock or ClockBoost circuitry		9.0		9.0		10.5	ns
t_{INREG} with ClockLock or ClockBoost circuitry		3.0		–		–	ns
t_{IOFD}		8.1		8.1		10.3	ns
t_{INCOMB}		8.1		8.1		10.3	ns

Table 67. EPF10K100 Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-3DX		-3		-4		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.5		1.9	ns
$t_{EABDATA2}$		4.8		4.8		6.0	ns
t_{EABWE1}		1.0		1.0		1.2	ns
t_{EABWE2}		5.0		5.0		6.2	ns
t_{EABCLK}		1.0		1.0		2.2	ns
t_{EABCO}		0.5		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.5		1.9	ns
t_{EABSU}	1.5		1.5		1.8		ns
t_{EABH}	2.0		2.0		2.5		ns
t_{AA}		8.7		8.7		10.7	ns
t_{WP}	5.8		5.8		7.2		ns
t_{WDSU}	1.6		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.5		0.5		0.6		ns
t_{WAH}	1.0		1.0		1.2		ns
t_{WO}		5.0		5.0		6.2	ns
t_{DD}		5.0		5.0		6.2	ns
t_{EABOUT}		0.5		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.8		5.8		7.2		ns

Table 68. EPF10K100 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade						Unit
	-3DX		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		13.7		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		13.7		17.0		ns
$t_{EABRCREG}$	9.7		9.7		11.9		ns
t_{EABWP}	5.8		5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		7.3		9.0		ns
$t_{EABWCREG}$	13.0		13.0		16.0		ns
t_{EABDD}		10.0		10.0		12.5	ns
$t_{EABDATACO}$		2.0		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	5.5		5.5		5.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.5		5.8		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.1		2.1		2.7		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		9.5		9.5		11.8	ns

Table 69. EPF10K100 Device Interconnect Timing Microparameters _Note (1)_							
Symbol	**Speed Grade**						**Unit**
	-3DX		**-3**		**-4**		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		10.3		10.3		12.2	ns
t_{DIN2LE}		4.8		4.8		6.0	ns
$t_{DIN2DATA}$		7.3		7.3		11.0	ns
$t_{DCLK2IOE}$ without ClockLock or ClockBoost circuitry		6.2		6.2		7.7	ns
$t_{DCLK2IOE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{DCLK2LE}$ without ClockLock or ClockBoost circuitry		4.8		4.8		6.0	ns
$t_{DCLK2LE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.9		4.9		5.5	ns
$t_{SAMECOLUMN}$		5.1		5.1		5.4	ns
$t_{DIFFROW}$		10.0		10.0		10.9	ns
$t_{TWOROWS}$		14.9		14.9		16.4	ns
$t_{LEPERIPH}$		6.9		6.9		8.1	ns
$t_{LABCARRY}$		0.9		0.9		1.1	ns
$t_{LABCASC}$		3.0		3.0		3.2	ns

Table 70. EPF10K100 Device External Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-3DX		**-3**		**-4**		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		19.1		19.1		24.2	ns
t_{INSU} *(2)*, *(3)*, *(4)*	7.8		7.8		8.5		ns
t_{OUTCO} *(3)*, *(4)*	2.0	11.1	2.0	11.1	2.0	14.3	ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{INSU} *(2)*, *(3)*, *(5)*	6.2						ns
t_{OUTCO} *(3)*, *(5)*	2.0	6.7		–		–	ns

Table 71. EPF10K100 Device External Bidirectional Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-3DX		**-3**		**-4**		
	Min	Max	Min	Max	Min	Max	
t_{INSUBIDIR} *(4)*	8.1		8.1		10.4		ns
t_{INHBIDIR} *(4)*	0.0		0.0		0.0		ns
t_{OUTCOBIDIR} *(4)*	2.0	11.1	2.0	11.1	2.0	14.3	ns
t_{XZBIDIR} *(4)*		15.3		15.3		18.4	ns
t_{ZXBIDIR} *(4)*		15.3		15.3		18.4	ns
t_{INSUBIDIR} *(5)*	9.1		–		–		ns
t_{INHBIDIR} *(5)*	0.0		–		–		ns
t_{OUTCOBIDIR} *(5)*	2.0	7.2	–	–	–	–	ns
t_{XZBIDIR} *(5)*		14.3		–		–	ns
t_{ZXBIDIR} *(5)*		14.3		–		–	ns

Notes to tables:
(1)   All timing parameters are described in Tables 32 through 39 in this data sheet.
(2)   Using an LE to register the signal may provide a lower setup time.
(3)   This parameter is specified by characterization.
(4)   This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(5)   This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 72 through 78 show EPF10K50V device internal and external timing parameters.

Table 72. EPF10K50V Device LE Timing Microparameters   *Note (1)*

Symbol	Speed Grade								Unit
	-1		-2		-3		-4		
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.0		1.3		1.6	ns
t_{CLUT}		0.1		0.5		0.6		0.6	ns
t_{RLUT}		0.5		0.8		0.9		1.0	ns
t_{PACKED}		0.4		0.4		0.5		0.7	ns
t_{EN}		0.7		0.9		1.1		1.4	ns
t_{CICO}		0.2		0.2		0.2		0.3	ns
t_{CGEN}		0.8		0.7		0.8		1.2	ns
t_{CGENR}		0.4		0.3		0.3		0.4	ns
t_{CASC}		0.7		0.7		0.8		0.9	ns
t_C		0.3		1.0		1.3		1.5	ns
t_{CO}		0.5		0.7		0.9		1.0	ns
t_{COMB}		0.4		0.4		0.5		0.6	ns
t_{SU}	0.8		1.6		2.2		2.5		ns
t_H	0.5		0.8		1.0		1.4		ns
t_{PRE}		0.8		0.4		0.5		0.5	ns
t_{CLR}		0.8		0.4		0.5		0.5	ns
t_{CH}	2.0		4.0		4.0		4.0		ns
t_{CL}	2.0		4.0		4.0		4.0		ns

Table 73. EPF10K50V Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade								Unit
	-1		-2		-3		-4		
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.2		1.6		1.9		2.1	ns
t_{IOC}		0.3		0.4		0.5		0.5	ns
t_{IOCO}		0.3		0.3		0.4		0.4	ns
t_{IOCOMB}		0.0		0.0		0.0		0.0	ns
t_{IOSU}	2.8		2.8		3.4		3.9		ns
t_{IOH}	0.7		0.8		1.0		1.4		ns
t_{IOCLR}		0.5		0.6		0.7		0.7	ns
t_{OD1}		2.8		3.2		3.9		4.7	ns
t_{OD2}		–		–		–		–	ns
t_{OD3}		6.5		6.9		7.6		8.4	ns
t_{XZ}		2.8		3.1		3.8		4.6	ns
t_{ZX1}		2.8		3.1		3.8		4.6	ns
t_{ZX2}		–		–		–		–	ns
t_{ZX3}		6.5		6.8		7.5		8.3	ns
t_{INREG}		5.0		5.7		7.0		9.0	ns
t_{IOFD}		1.5		1.9		2.3		2.7	ns
t_{INCOMB}		1.5		1.9		2.3		2.7	ns

Table 74. EPF10K50V Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade								Unit
	-1		-2		-3		-4		
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.8		3.4		4.6	ns
$t_{EABDATA2}$		4.9		3.9		4.8		5.9	ns
t_{EABWE1}		0.0		2.5		3.0		3.7	ns
t_{EABWE2}		4.0		4.1		5.0		6.2	ns
t_{EABCLK}		0.4		0.8		1.0		1.2	ns
t_{EABCO}		0.1		0.2		0.3		0.4	ns
$t_{EABBYPASS}$		0.9		1.1		1.3		1.6	ns
t_{EABSU}	0.8		1.5		1.8		2.2		ns
t_{EABH}	0.8		1.6		2.0		2.5		ns
t_{AA}		5.5		8.2		10.0		12.4	ns
t_{WP}	6.0		4.9		6.0		7.4		ns
t_{WDSU}	0.1		0.8		1.0		1.2		ns
t_{WDH}	0.1		0.2		0.3		0.4		ns
t_{WASU}	0.1		0.4		0.5		0.6		ns
t_{WAH}	0.1		0.8		1.0		1.2		ns
t_{WO}		2.8		4.3		5.3		6.5	ns
t_{DD}		2.8		4.3		5.3		6.5	ns
t_{EABOUT}		0.5		0.4		0.5		0.6	ns
t_{EABCH}	2.0		4.0		4.0		4.0		ns
t_{EABCL}	6.0		4.9		6.0		7.4		ns

Table 75. EPF10K50V Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	Speed Grade								Unit
	-1		-2		-3		-4		
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{EABAA}		9.5		13.6		16.5		20.8	ns
$t_{EABRCCOMB}$	9.5		13.6		16.5		20.8		ns
$t_{EABRCREG}$	6.1		8.8		10.8		13.4		ns
t_{EABWP}	6.0		4.9		6.0		7.4		ns
$t_{EABWCCOMB}$	6.2		6.1		7.5		9.2		ns
$t_{EABWCREG}$	12.0		11.6		14.2		17.4		ns
t_{EABDD}		6.8		9.7		11.8		14.9	ns
$t_{EABDATACO}$		1.0		1.4		1.8		2.2	ns
$t_{EABDATASU}$	5.3		4.6		5.6		6.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		0.0		ns
$t_{EABWESU}$	4.4		4.8		5.8		7.2		ns
t_{EABWEH}	0.0		0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.8		1.1		1.4		2.1		ns
t_{EABWDH}	0.0		0.0		0.0		0.0		ns
$t_{EABWASU}$	4.5		4.6		5.6		7.4		ns
t_{EABWAH}	0.0		0.0		0.0		0.0		ns
t_{EABWO}		5.1		9.4		11.4		14.0	ns

Table 76. EPF10K50V Device Interconnect Timing Microparameters   *Note (1)*

Symbol	Speed Grade								Unit
	-1		-2		-3		-4		
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.7		6.0		7.1		8.2	ns
t_{DIN2LE}		2.5		2.6		3.1		3.9	ns
$t_{DIN2DATA}$		4.4		5.9		6.8		7.7	ns
$t_{DCLK2IOE}$		2.5		3.9		4.7		5.5	ns
$t_{DCLK2LE}$		2.5		2.6		3.1		3.9	ns
$t_{SAMELAB}$		0.2		0.2		0.3		0.3	ns
$t_{SAMEROW}$		2.8		3.0		3.2		3.4	ns
$t_{SAMECOLUMN}$		3.0		3.2		3.4		3.6	ns
$t_{DIFFROW}$		5.8		6.2		6.6		7.0	ns
$t_{TWOROWS}$		8.6		9.2		9.8		10.4	ns
$t_{LEPERIPH}$		4.5		5.5		6.1		7.0	ns
$t_{LABCARRY}$		0.3		0.4		0.5		0.7	ns
$t_{LABCASC}$		0.0		1.3		1.6		2.0	ns

Table 77. EPF10K50V Device External Timing Parameters   *Note (1)*

Symbol	Speed Grade								Unit
	-1		-2		-3		-4		
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.2		14.0		17.2		21.1	ns
t_{INSU} *(2), (3)*	5.5		4.2		5.2		6.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns

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Table 78. EPF10K50V Device External Bidirectional Timing Parameters   *Note (1)*

Symbol	Speed Grade								Unit
	-1		-2		-3		-4		
	Min	Max	Min	Max	Min	Max	Min	Max	
t$_{INSUBIDIR}$	2.0		2.8		3.5		4.1		ns
t$_{INHBIDIR}$	0.0		0.0		0.0		0.0		ns
t$_{OUTCOBIDIR}$	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns
t$_{XZBIDIR}$		8.0		9.8		11.8		14.3	ns
t$_{ZXBIDIR}$		8.0		9.8		11.8		14.3	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 39 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 79 through 85 show EPF10K130V device internal and external timing parameters.

Table 79. EPF10K130V Device LE Timing Microparameters (Part 1 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-2		-3		-4		
	Min	Max	Min	Max	Min	Max	
t$_{LUT}$		1.3		1.8		2.3	ns
t$_{CLUT}$		0.5		0.7		0.9	ns
t$_{RLUT}$		1.2		1.7		2.2	ns
t$_{PACKED}$		0.5		0.6		0.7	ns
t$_{EN}$		0.6		0.8		1.0	ns
t$_{CICO}$		0.2		0.3		0.4	ns
t$_{CGEN}$		0.3		0.4		0.5	ns
t$_{CGENR}$		0.7		1.0		1.3	ns
t$_{CASC}$		0.9		1.2		1.5	ns
t$_C$		1.9		2.4		3.0	ns
t$_{CO}$		0.6		0.9		1.1	ns
t$_{COMB}$		0.5		0.7		0.9	ns
t$_{SU}$	0.2		0.2		0.3		ns
t$_H$	0.0		0.0		0.0		ns
t$_{PRE}$		2.4		3.1		3.9	ns
t$_{CLR}$		2.4		3.1		3.9	ns

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Table 79. EPF10K130V Device LE Timing Microparameters (Part 2 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 80. EPF10K130V Device IOE Timing Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.3		1.6		2.0	ns
t_{IOC}		0.4		0.5		0.7	ns
t_{IOCO}		0.3		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	2.6		3.3		3.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.7		2.2		2.7	ns
t_{OD1}		3.5		4.4		5.0	ns
t_{OD2}		–		–		–	ns
t_{OD3}		8.2		8.1		9.7	ns
t_{XZ}		4.9		6.3		7.4	ns
t_{ZX1}		4.9		6.3		7.4	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		9.6		10.0		12.1	ns
t_{INREG}		7.9		10.0		12.6	ns
t_{IOFD}		6.2		7.9		9.9	ns
t_{INCOMB}		6.2		7.9		9.9	ns

Table 81. EPF10K130V Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.9		2.4		2.4	ns
$t_{EABDATA2}$		3.7		4.7		4.7	ns
t_{EABWE1}		1.9		2.4		2.4	ns
t_{EABWE2}		3.7		4.7		4.7	ns
t_{EABCLK}		0.7		0.9		0.9	ns
t_{EABCO}		0.5		0.6		0.6	ns
$t_{EABBYPASS}$		0.6		0.8		0.8	ns
t_{EABSU}	1.4		1.8		1.8		ns
t_{EABH}	0.0		0.0		0.0		ns
t_{AA}		5.6		7.1		7.1	ns
t_{WP}	3.7		4.7		4.7		ns
t_{WDSU}	4.6		5.9		5.9		ns
t_{WDH}	0.0		0.0		0.0		ns
t_{WASU}	3.9		5.0		5.0		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		5.6		7.1		7.1	ns
t_{DD}		5.6		7.1		7.1	ns
t_{EABOUT}		2.4		3.1		3.1	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	4.0		4.7		4.7		ns

Table 82. EPF10K130V Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		11.2		14.2		14.2	ns
$t_{EABRCCOMB}$	11.1		14.2		14.2		ns
$t_{EABRCREG}$	8.5		10.8		10.8		ns
t_{EABWP}	3.7		4.7		4.7		ns
$t_{EABWCCOMB}$	7.6		9.7		9.7		ns
$t_{EABWCREG}$	14.0		17.8		17.8		ns
t_{EABDD}		11.1		14.2		14.2	ns
$t_{EABDATACO}$		3.6		4.6		4.6	ns
$t_{EABDATASU}$	4.4		5.6		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.4		5.6		5.6		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	4.6		5.9		5.9		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.9		5.0		5.0		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		11.1		14.2		14.2	ns

Table 83. EPF10K130V Device Interconnect Timing Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		-3		-4		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		8.0		9.0		9.5	ns
t_{DIN2LE}		2.4		3.0		3.1	ns
$t_{DIN2DATA}$		5.0		6.3		7.4	ns
$t_{DCLK2IOE}$		3.6		4.6		5.1	ns
$t_{DCLK2LE}$		2.4		3.0		3.1	ns
$t_{SAMELAB}$		0.4		0.6		0.8	ns
$t_{SAMEROW}$		4.5		5.3		6.5	ns
$t_{SAMECOLUMN}$		9.0		9.5		9.7	ns
$t_{DIFFROW}$		13.5		14.8		16.2	ns
$t_{TWOROWS}$		18.0		20.1		22.7	ns
$t_{LEPERIPH}$		8.1		8.6		9.5	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.8		1.0		1.2	ns

Table 84. EPF10K130V Device External Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		-3		-4		
	Min	Max	Min	Max	Min	Max	
t_DRR		15.0		19.1		24.2	ns
t_INSU *(2), (3)*	6.9		8.6		11.0		ns
t_INH *(3)*	0.0		0.0		0.0		ns
t_OUTCO *(3)*	2.0	7.8	2.0	9.9	2.0	11.3	ns

Table 85. EPF10K130V Device External Bidirectional Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$	6.7		8.5		10.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.9	2.0	8.8	2.0	10.2	ns
$t_{XZBIDIR}$		12.9		16.4		19.3	ns
$t_{ZXBIDIR}$		12.9		16.4		19.3	ns

Notes to tables:
(1)   All timing parameters are described in Tables 32 through 39 in this data sheet.
(2)   Using an LE to register the signal may provide a lower setup time.
(3)   This parameter is specified by characterization.

Tables 86 through 92 show EPF10K10A device internal and external timing parameters.

Table 86. EPF10K10A Device LE Timing Microparameters (Part 1 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		0.9		1.2		1.6	ns
t_{CLUT}		1.2		1.4		1.9	ns
t_{RLUT}		1.9		2.3		3.0	ns
t_{PACKED}		0.6		0.7		0.9	ns
t_{EN}		0.5		0.6		0.8	ns
t_{CICO}		02		0.3		0.4	ns
t_{CGEN}		0.7		0.9		1.1	ns
t_{CGENR}		0.7		0.9		1.1	ns
t_{CASC}		1.0		1.2		1.7	ns
t_C		1.2		1.4		1.9	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.5		0.6		0.8	ns
t_{SU}	1.1		1.3		1.7		ns
t_H	0.6		0.7		0.9		ns
t_{PRE}		0.5		0.6		0.9	ns
t_{CLR}		0.5		0.6		0.9	ns

Table 86. EPF10K10A Device LE Timing Microparameters (Part 2 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
t_{CH}	3.0		3.5		4.0		ns
t_{CL}	3.0		3.5		4.0		ns

Table 87. EPF10K10A Device IOE Timing Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.3		1.5		2.0	ns
t_{IOC}		0.2		0.3		0.3	ns
t_{IOCO}		0.2		0.3		0.4	ns
t_{IOCOMB}		0.6		0.7		0.9	ns
t_{IOSU}	0.8		1.0		1.3		ns
t_{IOH}	0.8		1.0		1.3		ns
t_{IOCLR}		1.2		1.4		1.9	ns
t_{OD1}		1.2		1.4		1.9	ns
t_{OD2}		2.9		3.5		4.7	ns
t_{OD3}		6.6		7.8		10.5	ns
t_{XZ}		1.2		1.4		1.9	ns
t_{ZX1}		1.2		1.4		1.9	ns
t_{ZX2}		2.9		3.5		4.7	ns
t_{ZX3}		6.6		7.8		10.5	ns
t_{INREG}		5.2		6.3		8.4	ns
t_{IOFD}		3.1		3.8		5.0	ns
t_{INCOMB}		3.1		3.8		5.0	ns

Table 88. EPF10K10A Device EAB Internal Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		3.3		3.9		5.2	ns
$t_{EABDATA2}$		1.0		1.3		1.7	ns
t_{EABWE1}		2.6		3.1		4.1	ns
t_{EABWE2}		2.7		3.2		4.3	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		1.2		1.4		1.8	ns
$t_{EABBYPASS}$		0.1		0.2		0.2	ns
t_{EABSU}	1.4		1.7		2.2		ns
t_{EABH}	0.1		0.1		0.1		ns
t_{AA}		4.5		5.4		7.3	ns
t_{WP}	2.0		2.4		3.2		ns
t_{WDSU}	0.7		0.8		1.1		ns
t_{WDH}	0.5		0.6		0.7		ns
t_{WASU}	0.6		0.7		0.9		ns
t_{WAH}	0.9		1.1		1.5		ns
t_{WO}		3.3		3.9		5.2	ns
t_{DD}		3.3		3.9		5.2	ns
t_{EABOUT}		0.1		0.1		0.2	ns
t_{EABCH}	3.0		3.5		4.0		ns
t_{EABCL}	3.03		3.5		4.0		ns

Table 89. EPF10K10A Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		8.1		9.8		13.1	ns
$t_{EABRCCOMB}$	8.1		9.8		13.1		ns
$t_{EABRCREG}$	5.8		6.9		9.3		ns
t_{EABWP}	2.0		2.4		3.2		ns
$t_{EABWCCOMB}$	3.5		4.2		5.6		ns
$t_{EABWCREG}$	9.4		11.2		14.8		ns
t_{EABDD}		6.9		8.3		11.0	ns
$t_{EABDATACO}$		1.3		1.5		2.0	ns
$t_{EABDATASU}$	2.4		3.0		3.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.1		4.9		6.5		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.4		1.6		2.2		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.5		3.0		4.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.2		7.5		9.9	ns

Table 90. EPF10K10A Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.2		5.0		6.5	ns
t_{DIN2LE}		2.2		2.6		3.4	ns
$t_{DIN2DATA}$		4.3		5.2		7.1	ns
$t_{DCLK2IOE}$		4.2		4.9		6.6	ns
$t_{DCLK2LE}$		2.2		2.6		3.4	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.2		2.4		2.9	ns
$t_{SAMECOLUMN}$		0.8		1.0		1.4	ns
$t_{DIFFROW}$		3.0		3.4		4.3	ns
$t_{TWOROWS}$		5.2		5.8		7.2	ns
$t_{LEPERIPH}$		1.8		2.2		2.8	ns
$t_{LABCARRY}$		0.5		0.5		0.7	ns
$t_{LABCASC}$		0.9		1.0		1.5	ns

Table 91. EPF10K10A External Reference Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		10.0		12.0		16.0	ns
t_{INSU} *(2)*, *(3)*	1.6		2.1		2.8		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.8	2.0	6.9	2.0	9.2	ns

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Table 92. EPF10K10A Device External Bidirectional Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-2		**-3**		**-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t$_{INSUBIDIR}$	2.4		3.3		4.5		ns
t$_{INHBIDIR}$	0.0		0.0		0.0		ns
t$_{OUTCOBIDIR}$	2.0	5.8	2.0	6.9	2.0	9.2	ns
t$_{XZBIDIR}$		6.3		7.5		9.9	ns
t$_{ZXBIDIR}$		6.3		7.5		9.9	ns

Notes to tables:
(1)   All timing parameters are described in Tables 32 through 39 in this data sheet.
(2)   Using an LE to register the signal may provide a lower setup time.
(3)   This parameter is specified by characterization.

Tables 93 through 99 show EPF10K30A device internal and external timing parameters.

Table 93. EPF10K30A Device LE Timing Microparameters (Part 1 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t$_{LUT}$		0.8		1.1		1.5	ns
t$_{CLUT}$		0.6		0.7		1.0	ns
t$_{RLUT}$		1.2		1.5		2.0	ns
t$_{PACKED}$		0.6		0.6		1.0	ns
t$_{EN}$		1.3		1.5		2.0	ns
t$_{CICO}$		0.2		0.3		0.4	ns
t$_{CGEN}$		0.8		1.0		1.3	ns
t$_{CGENR}$		0.6		0.8		1.0	ns
t$_{CASC}$		0.9		1.1		1.4	ns
t$_{C}$		1.1		1.3		1.7	ns
t$_{CO}$		0.4		0.6		0.7	ns
t$_{COMB}$		0.6		0.7		0.9	ns
t$_{SU}$	0.9		0.9		1.4		ns
t$_{H}$	1.1		1.3		1.7		ns
t$_{PRE}$		0.5		0.6		0.8	ns
t$_{CLR}$		0.5		0.6		0.8	ns

Table 93. EPF10K30A Device LE Timing Microparameters (Part 2 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{CH}	3.0		3.5		4.0		ns
t_{CL}	3.0		3.5		4.0		ns

Table 94. EPF10K30A Device IOE Timing Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.2		2.6		3.4	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		0.2		0.2		0.3	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	1.4		1.7		2.2		ns
t_{IOH}	0.9		1.1		1.4		ns
t_{IOCLR}		0.7		0.8		1.0	ns
t_{OD1}		1.9		2.2		2.9	ns
t_{OD2}		4.8		5.6		7.3	ns
t_{OD3}		7.0		8.2		10.8	ns
t_{XZ}		2.2		2.6		3.4	ns
t_{ZX1}		2.2		2.6		3.4	ns
t_{ZX2}		5.1		6.0		7.8	ns
t_{ZX3}		7.3		8.6		11.3	ns
t_{INREG}		4.4		5.2		6.8	ns
t_{IOFD}		3.8		4.5		5.9	ns
t_{INCOMB}		3.8		4.5		5.9	ns

Table 95. EPF10K30A Device EAB Internal Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		5.5		6.5		8.5	ns
$t_{EABDATA2}$		1.1		1.3		1.8	ns
t_{EABWE1}		2.4		2.8		3.7	ns
t_{EABWE2}		2.1		2.5		3.2	ns
t_{EABCLK}		0.0		0.0		0.2	ns
t_{EABCO}		1.7		2.0		2.6	ns
$t_{EABBYPASS}$		0.0		0.0		0.3	ns
t_{EABSU}	1.2		1.4		1.9		ns
t_{EABH}	0.1		0.1		0.3		ns
t_{AA}		4.2		5.0		6.5	ns
t_{WP}	3.8		4.5		5.9		ns
t_{WDSU}	0.1		0.1		0.2		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	0.1		0.1		0.2		ns
t_{WAH}	0.1		0.1		0.2		ns
t_{WO}		3.7		4.4		6.4	ns
t_{DD}		3.7		4.4		6.4	ns
t_{EABOUT}		0.0		0.1		0.6	ns
t_{EABCH}	3.0		3.5		4.0		ns
t_{EABCL}	3.8		4.5		5.9		ns

Table 96. EPF10K30A Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		9.7		11.6		16.2	ns
$t_{EABRCCOMB}$	9.7		11.6		16.2		ns
$t_{EABRCREG}$	5.9		7.1		9.7		ns
t_{EABWP}	3.8		4.5		5.9		ns
$t_{EABWCCOMB}$	4.0		4.7		6.3		ns
$t_{EABWCREG}$	9.8		11.6		16.6		ns
t_{EABDD}		9.2		11.0		16.1	ns
$t_{EABDATACO}$		1.7		2.1		3.4	ns
$t_{EABDATASU}$	2.3		2.7		3.5		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	3.3		3.9		4.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.2		3.8		5.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.7		4.4		5.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.1		7.3		11.3	ns

Table 97. EPF10K30A Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.9		4.4		5.1	ns
t_{DIN2LE}		1.2		1.5		1.9	ns
$t_{DIN2DATA}$		3.2		3.6		4.5	ns
$t_{DCLK2IOE}$		3.0		3.5		4.6	ns
$t_{DCLK2LE}$		1.2		1.5		1.9	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.3		2.4		2.7	ns
$t_{SAMECOLUMN}$		1.3		1.4		1.9	ns
$t_{DIFFROW}$		3.6		3.8		4.6	ns
$t_{TWOROWS}$		5.9		6.2		7.3	ns
$t_{LEPERIPH}$		3.5		3.8		4.1	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.9		1.1		1.4	ns

Table 98. EPF10K30A External Reference Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.0		13.0		17.0	ns
t_{INSU} *(2), (3)*	2.5		3.1		3.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.4	2.0	6.2	2.0	8.3	ns

Table 99. EPF10K30A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.2		4.9		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.4	2.0	6.2	2.0	8.3	ns
$t_{XZBIDIR}$		6.2		7.5		9.8	ns
$t_{ZXBIDIR}$		6.2		7.5		9.8	ns

Notes to tables:
(1)   All timing parameters are described in Tables 32 through 39 in this data sheet.
(2)   Using an LE to register the signal may provide a lower setup time.
(3)   This parameter is specified by characterization.

Tables 100 through 106 show EPF10K100A device internal and external timing parameters.

Table 100. EPF10K100A Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.0		1.2		1.4	ns
t_{CLUT}		0.8		0.9		1.1	ns
t_{RLUT}		1.4		1.6		1.9	ns
t_{PACKED}		0.4		0.5		0.5	ns
t_{EN}		0.6		0.7		0.8	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.4		0.4		0.6	ns
t_{CGENR}		0.6		0.7		0.8	ns
t_{CASC}		0.7		0.9		1.0	ns
t_C		0.9		1.0		1.2	ns
t_{CO}		0.2		0.3		0.3	ns
t_{COMB}		0.6		0.7		0.8	ns
t_{SU}	0.8		1.0		1.2		ns
t_H	0.3		0.5		0.5		ns
t_{PRE}		0.3		0.3		0.4	ns
t_{CLR}		0.3		0.3		0.4	ns

Table 100. EPF10K100A Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{CH}	2.5		3.5		4.0		ns
t_{CL}	2.5		3.5		4.0		ns

Table 101. EPF10K100A Device IOE Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		2.5		2.9		3.4	ns
t_{IOC}		0.3		0.3		0.4	ns
t_{IOCO}		0.2		0.2		0.3	ns
t_{IOCOMB}		0.5		0.6		0.7	ns
t_{IOSU}	1.3		1.7		1.8		ns
t_{IOH}	0.2		0.2		0.3		ns
t_{IOCLR}		1.0		1.2		1.4	ns
t_{OD1}		2.2		2.6		3.0	ns
t_{OD2}		4.5		5.3		6.1	ns
t_{OD3}		6.8		7.9		9.3	ns
t_{XZ}		2.7		3.1		3.7	ns
t_{ZX1}		2.7		3.1		3.7	ns
t_{ZX2}		5.0		5.8		6.8	ns
t_{ZX3}		7.3		8.4		10.0	ns
t_{INREG}		5.3		6.1		7.2	ns
t_{IOFD}		4.7		5.5		6.4	ns
t_{INCOMB}		4.7		5.5		6.4	ns

Table 102. EPF10K100A Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.8		2.1		2.4	ns
$t_{EABDATA2}$		3.2		3.7		4.4	ns
t_{EABWE1}		0.8		0.9		1.1	ns
t_{EABWE2}		2.3		2.7		3.1	ns
t_{EABCLK}		0.8		0.9		1.1	ns
t_{EABCO}		1.0		1.1		1.4	ns
$t_{EABBYPASS}$		0.3		0.3		0.4	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	0.4		0.5		0.5		ns
t_{AA}		4.1		4.8		5.6	ns
t_{WP}	3.2		3.7		4.4		ns
t_{WDSU}	2.4		2.8		3.3		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	0.2		0.2		0.3		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		3.4		3.9		4.6	ns
t_{DD}		3.4		3.9		4.6	ns
t_{EABOUT}		0.3		0.3		0.4	ns
t_{EABCH}	2.5		3.5		4.0		ns
t_{EABCL}	3.2		3.7		4.4		ns

Table 103. EPF10K100A Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.8		7.8		9.2	ns
$t_{EABRCCOMB}$	6.8		7.8		9.2		ns
$t_{EABRCREG}$	5.4		6.2		7.4		ns
t_{EABWP}	3.2		3.7		4.4		ns
$t_{EABWCCOMB}$	3.4		3.9		4.7		ns
$t_{EABWCREG}$	9.4		10.8		12.8		ns
t_{EABDD}		6.1		6.9		8.2	ns
$t_{EABDATACO}$		2.1		2.3		2.9	ns
$t_{EABDATASU}$	3.7		4.3		5.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	2.8		3.3		3.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.4		4.0		4.6		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.9		2.3		2.6		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		5.1		5.7		6.9	ns

Table 104. EPF10K100A Device Interconnect Timing Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.8		5.4		6.0	ns
t_{DIN2LE}		2.0		2.4		2.7	ns
$t_{DIN2DATA}$		2.4		2.7		2.9	ns
$t_{DCLK2IOE}$		2.6		3.0		3.5	ns
$t_{DCLK2LE}$		2.0		2.4		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.1	ns
$t_{SAMEROW}$		1.5		1.7		1.9	ns
$t_{SAMECOLUMN}$		5.5		6.5		7.4	ns
$t_{DIFFROW}$		7.0		8.2		9.3	ns
$t_{TWOROWS}$		8.5		9.9		11.2	ns
$t_{LEPERIPH}$		3.9		4.2		4.5	ns
$t_{LABCARRY}$		0.2		0.2		0.3	ns
$t_{LABCASC}$		0.4		0.5		0.6	ns

Table 105. EPF10K100A Device External Timing Parameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		12.5		14.5		17.0	ns
t_{INSU} *(2), (3)*	3.7		4.5		5.1		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.3	2.0	6.1	2.0	7.2	ns

Table 106. EPF10K100A Device External Bidirectional Timing Parameters   Note (1)

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.9		5.8		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.3	2.0	6.1	2.0	7.2	ns
$t_{XZBIDIR}$		7.4		8.6		10.1	ns
$t_{ZXBIDIR}$		7.4		8.6		10.1	ns

Notes to tables:
(1)   All timing parameters are described in Tables 32 through 39 in this data sheet.
(2)   Using an LE to register the signal may provide a lower setup time.
(3)   This parameter is specified by characterization.

Tables 107 through 113 show EPF10K250A device internal and external timing parameters.

Table 107. EPF10K250A Device LE Timing Microparameters (Part 1 of 2)   Note (1)

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.0		1.4	ns
t_{CLUT}		1.2		1.3		1.6	ns
t_{RLUT}		2.0		2.3		2.7	ns
t_{PACKED}		0.4		0.4		0.5	ns
t_{EN}		1.4		1.6		1.9	ns
t_{CICO}		0.2		0.3		0.3	ns
t_{CGEN}		0.4		0.6		0.6	ns
t_{CGENR}		0.8		1.0		1.1	ns
t_{CASC}		0.7		0.8		1.0	ns
t_C		1.2		1.3		1.6	ns
t_{CO}		0.6		0.7		0.9	ns
t_{COMB}		0.5		0.6		0.7	ns
t_{SU}	1.2		1.4		1.7		ns
t_H	1.2		1.3		1.6		ns
t_{PRE}		0.7		0.8		0.9	ns
t_{CLR}		0.7		0.8		0.9	ns

Table 107. EPF10K250A Device LE Timing Microparameters (Part 2 of 2)   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 108. EPF10K250A Device IOE Timing Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.2		1.3		1.6	ns
t_{IOC}		0.4		0.4		0.5	ns
t_{IOCO}		0.8		0.9		1.1	ns
t_{IOCOMB}		0.7		0.7		0.8	ns
t_{IOSU}	2.7		3.1		3.6		ns
t_{IOH}	0.2		0.3		0.3		ns
t_{IOCLR}		1.2		1.3		1.6	ns
t_{OD1}		3.2		3.6		4.2	ns
t_{OD2}		5.9		6.7		7.8	ns
t_{OD3}		8.7		9.8		11.5	ns
t_{XZ}		3.8		4.3		5.0	ns
t_{ZX1}		3.8		4.3		5.0	ns
t_{ZX2}		6.5		7.4		8.6	ns
t_{ZX3}		9.3		10.5		12.3	ns
t_{INREG}		8.2		9.3		10.9	ns
t_{IOFD}		9.0		10.2		12.0	ns
t_{INCOMB}		9.0		10.2		12.0	ns

Table 109. EPF10K250A Device EAB Internal Microparameters *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.3		1.5		1.7	ns
$t_{EABDATA2}$		1.3		1.5		1.7	ns
t_{EABWE1}		0.9		1.1		1.3	ns
t_{EABWE2}		5.0		5.7		6.7	ns
t_{EABCLK}		0.6		0.7		0.8	ns
t_{EABCO}		0.0		0.0		0.0	ns
$t_{EABBYPASS}$		0.1		0.1		0.2	ns
t_{EABSU}	3.8		4.3		5.0		ns
t_{EABH}	0.7		0.8		0.9		ns
t_{AA}		4.5		5.0		5.9	ns
t_{WP}	5.6		6.4		7.5		ns
t_{WDSU}	1.3		1.4		1.7		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	0.1		0.1		0.2		ns
t_{WAH}	0.1		0.1		0.2		ns
t_{WO}		4.1		4.6		5.5	ns
t_{DD}		4.1		4.6		5.5	ns
t_{EABOUT}		0.1		0.1		0.2	ns
t_{EABCH}	2.5		3.0		3.5		ns
t_{EABCL}	5.6		6.4		7.5		ns

Table 110. EPF10K250A Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		6.1		6.8		8.2	ns
$t_{EABRCCOMB}$	6.1		6.8		8.2		ns
$t_{EABRCREG}$	4.6		5.1		6.1		ns
t_{EABWP}	5.6		6.4		7.5		ns
$t_{EABWCCOMB}$	5.8		6.6		7.9		ns
$t_{EABWCREG}$	15.8		17.8		21.0		ns
t_{EABDD}		5.7		6.4		7.8	ns
$t_{EABDATACO}$		0.7		0.8		1.0	ns
$t_{EABDATASU}$	4.5		5.1		5.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	8.2		9.3		10.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.7		1.8		2.1		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	0.9		0.9		1.0		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		5.3		6.0		7.4	ns

Table 111. EPF10K250A Device Interconnect Timing Microparameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.8		8.5		9.4	ns
t_{DIN2LE}		2.7		3.1		3.5	ns
$t_{DIN2DATA}$		1.6		1.6		1.7	ns
$t_{DCLK2IOE}$		3.6		4.0		4.6	ns
$t_{DCLK2LE}$		2.7		3.1		3.5	ns
$t_{SAMELAB}$		0.2		0.3		0.3	ns
$t_{SAMEROW}$		6.7		7.3		8.2	ns
$t_{SAMECOLUMN}$		2.5		2.7		3.0	ns
$t_{DIFFROW}$		9.2		10.0		11.2	ns
$t_{TWOROWS}$		15.9		17.3		19.4	ns
$t_{LEPERIPH}$		7.5		8.1		8.9	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.4		0.4		0.5	ns

Table 112. EPF10K250A Device External Reference Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		15.0		17.0		20.0	ns
t_{INSU} (2), (3)	6.9		8.0		9.4		ns
t_{INH} (3)	0.0		0.0		0.0		ns
t_{OUTCO} (3)	2.0	8.0	2.0	8.9	2.0	10.4	ns

Table 113. EPF10K250A Device External Bidirectional Timing Parameters   *Note (1)*

Symbol	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$	9.3		10.6		12.7		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	8.0	2.0	8.9	2.0	10.4	ns
$t_{XZBIDIR}$		10.8		12.2		14.2	ns
$t_{ZXBIDIR}$		10.8		12.2		14.2	ns

Notes to tables:
(1)   All timing parameters are described in Tables 32 through 38 in this data sheet.
(2)   Using an LE to register the signal may provide a lower setup time.
(3)   This parameter is specified by characterization.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 31 illustrates the incoming and generated clock specifications.

Figure 31. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.
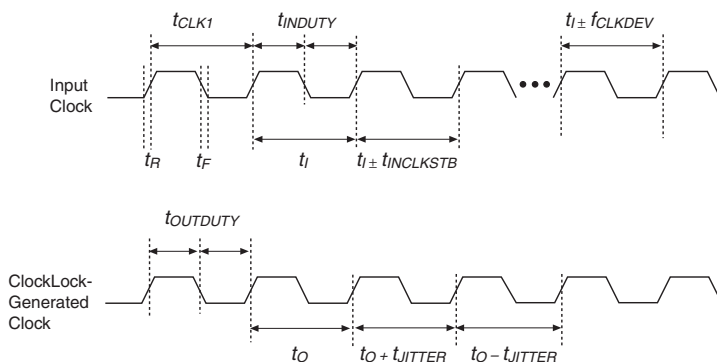
Table 114 summarizes the ClockLock and ClockBoost parameters.

Table 114. ClockLock & ClockBoost Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_R	Input rise time			2	ns
t_F	Input fall time			2	ns
t_{INDUTY}	Input duty cycle	45		55	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	30		80	MHz
t_{CLK1}	Input clock period (ClockBoost clock multiplication factor equals 1)	12.5		33.3	ns
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16		50	MHz
t_{CLK2}	Input clock period (ClockBoost clock multiplication factor equals 2)	20		62.5	ns
$f_{CLKDEV1}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 1) (1)			±1	MHz
$f_{CLKDEV2}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 2) (1)			±0.5	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (2)			10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (3)			1	ns
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock	40	50	60	%

Notes:
(1)   To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The MAX+PLUS II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.
(2)   During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the t_{LOCK} value is less than the time required for configuration.
(3)   The t_{JITTER} specification is measured under long-term observation.

Power Consumption

The supply power (P) for FLEX 10K devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the FLEX 10K device DC operating conditions tables on pages 44, 47, and 50 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

☞ Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times tog_{LC} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below:

f_{MAX}	=	Maximum operating frequency in MHz
N	=	Total number of logic cells used in the device
tog_{LC}	=	Average percent of logic cells toggling at each clock (typically 12.5%)
K	=	Constant, shown in Tables 115 and 116

Table 115. FLEX 10K K Constant Values

Device	K Value
EPF10K10	82
EPF10K20	89
EPF10K30	88
EPF10K40	92
EPF10K50	95
EPF10K70	85
EPF10K100	88

Table 116. FLEX 10KA K Constant Values

Device	K Value
EPF10K10A	17
EPF10K30A	17
EPF10K50V	19
EPF10K100A	19
EPF10K130V	22
EPF10K250A	23

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

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To better reflect actual designs, the power model (and the constant *K* in the power calculation equations) for continuous interconnect FLEX devices assumes that logic cells drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all logic cells drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

Figure 32 shows the relationship between the current and operating frequency of FLEX 10K devices.

Figure 32. I$_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 3)

EPF10K10
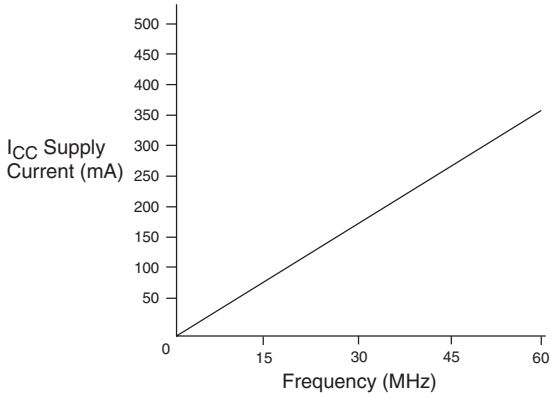
EPF10K20
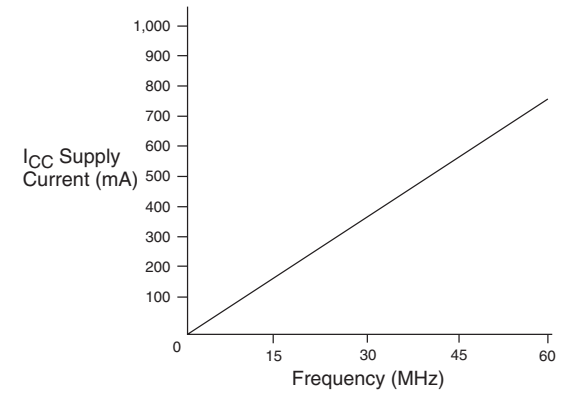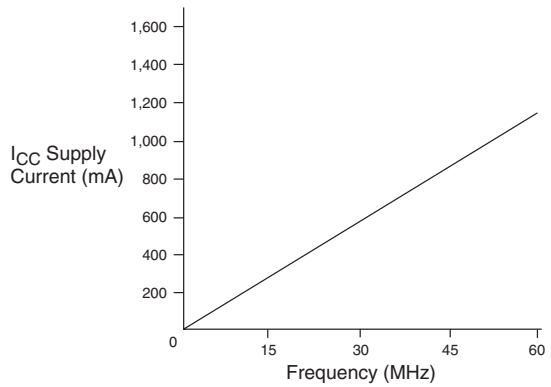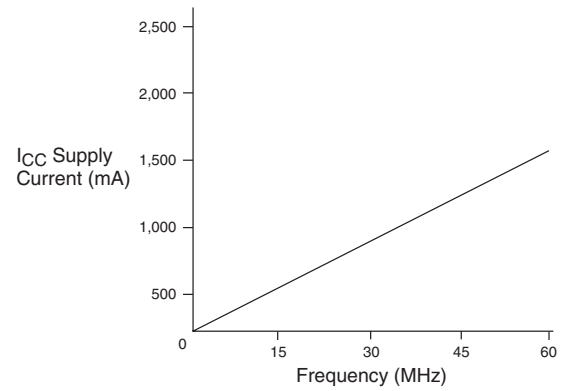
EPF10K30
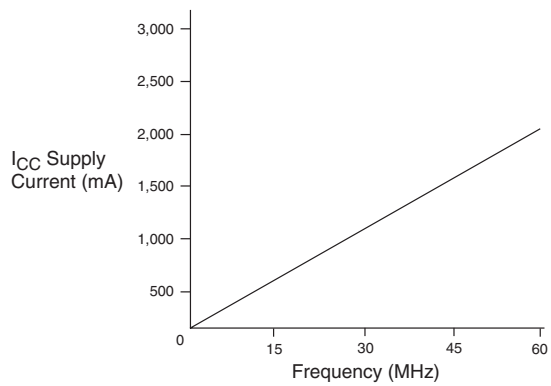
EPF10K40
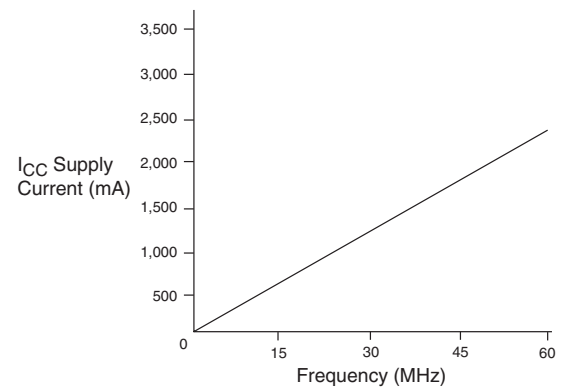
EPF10K50

EPF10K70

Figure 32. $I_{CCACTIVE}$ vs. Operating Frequency (Part 2 of 3)

EPF10K100
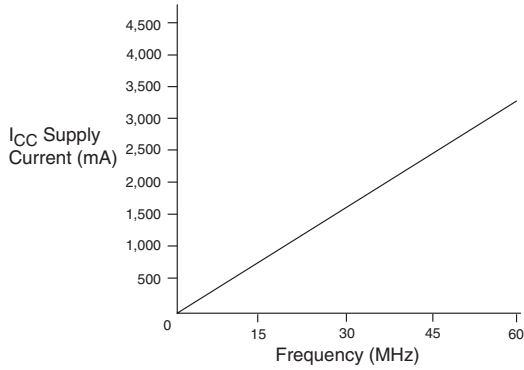
EPF10K50V
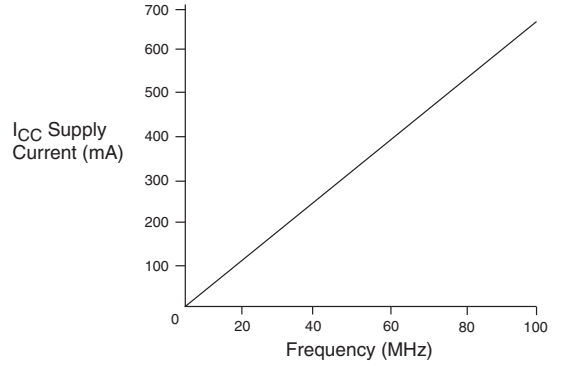
EPF10K130V
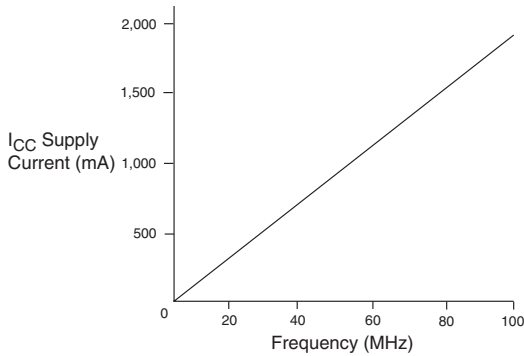
EPF10K10A
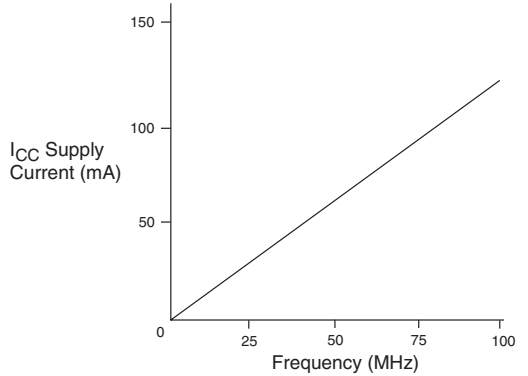
EPF10K30A
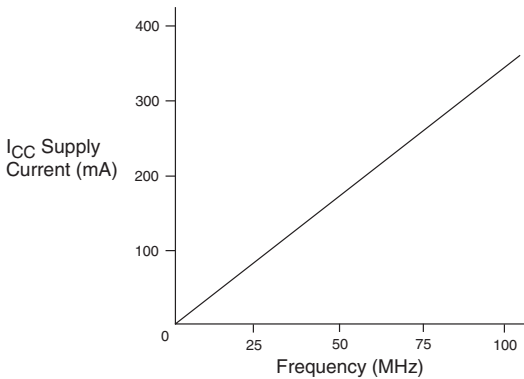
EPF10K100A
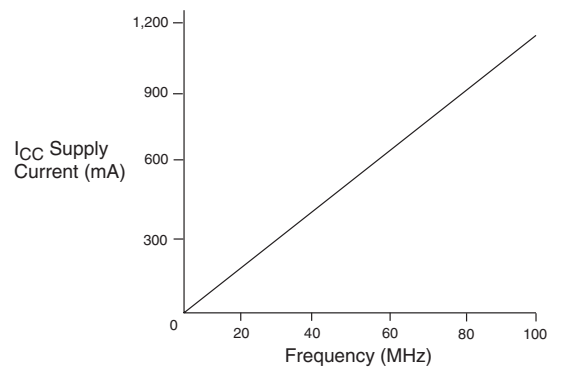
Figure 32. I_{CCACTIVE} vs. Operating Frequency (Part 3 of 3)

EPF10K250A
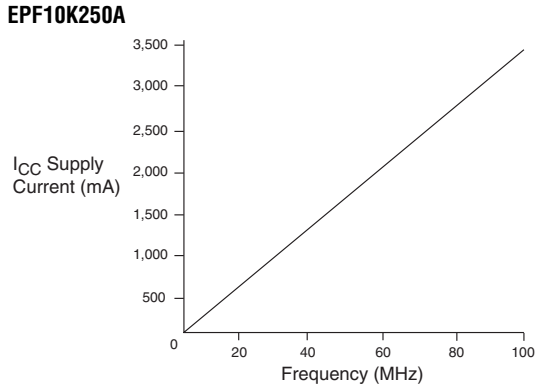
Configuration & Operation

The FLEX 10K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

See *Application Note 59 (Configuring FLEX 10K Devices)* for detailed descriptions of device configuration options, device configuration pins, and for information on configuring FLEX 10K devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 10K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation.

The entire reconfiguration process may be completed in less than 320 ms using an EPF10K250A device with a DCLK frequency of 10 MHz. This process can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Programming Files

Despite being function- and pin-compatible, FLEX 10KA and FLEX 10KE devices are not programming- or configuration-file compatible with FLEX 10K devices. A design should be recompiled before it is transferred from a FLEX 10K device to an equivalent FLEX 10KA or FLEX 10KE device. This recompilation should be performed to create a new programming or configuration file and to check design timing on the faster FLEX 10KA or FLEX 10KE device. The programming or configuration files for EPF10K50 devices can program or configure an EPF10K50V device. However, Altera recommends recompiling a design for the EPF10K50V device when transferring it from the EPF10K50 device.

Configuration Schemes

The configuration data for a FLEX 10K device can be loaded with one of five configuration schemes (see Table 117), chosen on the basis of the target application. An EPC2, EPC1, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10K device, allowing automatic configuration on system power-up.

Multiple FLEX 10K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 117. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC2, EPC1, or EPC1441 configuration device
Passive serial (PS)	BitBlaster, ByteBlaster, or ByteBlasterMV download cable, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster, ByteBlaster, or ByteBlasterMV download cable, or microprocessor with Jam File or Jam Byte-Code File

Device Pin-Outs

Tables 118 through 122 show the pin names and numbers for the dedicated pins in each FLEX 10K device package.

Table 118. FLEX 10K Device Pin-Outs (Part 1 of 2)   *Note (1)*

Pin Name	84-Pin PLCC EPF10K10	100-Pin TQFP EPF10K10A	144-Pin TQFP EPF10K10 EPF10K10A EPF10K20 EPF10K30A	208-Pin PQFP/RQFP EPF10K10 EPF10K10A	208-Pin PQFP/ RQFP EPF10K20 EPF10K30 EPF10K30A EPF10K40
MSEL0 (2)	31	54	77	108	108
MSEL1 (2)	32	53	76	107	107
nSTATUS (2)	55	25	35	52	52
nCONFIG (2)	34	51	74	105	105
DCLK (2)	13	75	107	155	155
CONF_DONE (2)	76	1	2	2	2
INIT_DONE (3)	69	10	14	19	19
nCE (2)	14	74	106	154	154
nCEO (2)	75	2	3	3	3
nWS (4)	80	97	142	206	206
nRS (4)	81	96	141	204	204
nCS (4)	78	99	144	208	208
CS (4)	79	98	143	207	207
RDYnBSY (4)	70	8	11	16	16
CLKUSR (4)	73	5	7	10	10
DATA7 (4)	5	84	116	166	166
DATA6 (4)	6	82	114	164	164
DATA5 (4)	7	81	113	162	162
DATA4 (4)	8	80	112	161	161
DATA3 (4)	9	79	111	159	159
DATA2 (4)	10	78	110	158	158
DATA1 (4)	11	77	109	157	157
DATA0 (2), (5)	12	76	108	156	156
TDI (2)	15	73	105	153	153
TDO (2)	74	3	4	4	4
TCK (2)	77	100	1	1	1
TMS (2)	57	24	34	50	50
TRST (2)	56	(6)	(6)	51	51
Dedicated Inputs	2, 42, 44, 84	40, 38, 89, 91	54, 56, 124, 126	78, 80, 182, 184	78, 80, 182, 184

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Table 118. FLEX 10K Device Pin-Outs (Part 2 of 2)   Note (1)

Pin Name	84-Pin PLCC EPF10K10	100-Pin TQFP EPF10K10A	144-Pin TQFP EPF10K10 EPF10K10A EPF10K20 EPF10K30A	208-Pin PQFP/RQFP EPF10K10 EPF10K10A	208-Pin PQFP/ RQFP EPF10K20 EPF10K30 EPF10K30A EPF10K40
Dedicated Clock Pins	1, 43	39, 90	55, 125	79, 183	79, 183
DEV_CLRn (3)	3	87	122	180	180
DEV_OE (3)	83	93	128	186	186
VCCINT	4, 20, 33, 40, 45, 63	18, 37, 52, 66, 88	6, 25, 52, 53, 75, 93, 123	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181
VCCIO	–	4, 17, 32, 49, 67, 83	5, 24, 45, 61, 71, 94, 115, 134	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194
GNDINT	26, 41, 46, 68, 82	12, 41, 59, 92	16, 57, 58, 84, 103, 127	21, 33, 49, 81, 82, 123, 129, 151, 185	21, 33, 49, 81, 82, 123, 129, 151, 185
GNDIO	–	11, 28, 46, 60, 72, 95	15, 40, 50, 66, 85, 104, 129, 139	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201
No Connect (N.C.) (7)	–	–	–	7, 8, 9, 14, 15, 36, 37, 113, 114, 125, 126, 139, 140	–
Total User I/O Pins (8)	59	66	102	134	147

Table 119. FLEX 10K Device Pin-Outs (Part 1 of 2)   *Note (1)*

Pin Name	240-Pin PQFP/RQFP EPF10K20 EPF10K30 EPF10K30A EPF10K40 EPF10K50 EPF10K50V EPF10K70 EPF10K100A	256-Pin FineLine BGA EPF10K10A	256-Pin FineLine BGA EPF10K30A
MSEL0 *(2)*	124	P1	P1
MSEL1 *(2)*	123	R1	R1
nSTATUS *(2)*	60	T16	T16
nCONFIG *(2)*	121	N4	N4
DCLK *(2)*	179	B2	B2
CONF_DONE *(2)*	2	C15	C15
INIT_DONE *(3)*	26	G16	G16
nCE *(2)*	178	B1	B1
nCEO *(2)*	3	B16	B16
nWS *(4)*	238	B14	B14
nRS *(4)*	236	C14	C14
nCS *(4)*	240	A16	A16
CS *(4)*	239	A15	A15
RDYnBSY *(4)*	23	G14	G14
CLKUSR *(4)*	11	D15	D15
DATA7 *(4)*	190	B5	B5
DATA6 *(4)*	188	D4	D4
DATA5 *(4)*	186	A4	A4
DATA4 *(4)*	185	B4	B4
DATA3 *(4)*	183	C3	C3
DATA2 *(4)*	182	A2	A2
DATA1 *(4)*	181	B3	B3
DATA0 *(2)*, *(5)*	180	A1	A1
TDI *(2)*	177	C2	C2
TDO *(2)*	4	C16	C16
TCK *(2)*	1	B15	B15
TMS *(2)*	58	P15	P15
TRST *(2)*	59	R16	R16
Dedicated Inputs	90, 92, 210, 212	B9, E8, M9, R8	B9, E8, M9, R8

Table 119. FLEX 10K Device Pin-Outs (Part 2 of 2)   *Note (1)*

Pin Name	240-Pin PQFP/RQFP EPF10K20 EPF10K30 EPF10K30A EPF10K40 EPF10K50 EPF10K50V EPF10K70 EPF10K100A	256-Pin FineLine BGA EPF10K10A	256-Pin FineLine BGA EPF10K30A
Dedicated Clock Pins	91, 211	A9, L8	A9, L8
DEV_CLRn *(3)*	209	D8	D8
DEV_OE *(3)*	213	C9	C9
VCCINT	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L9, L12, M11, R2	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L9, L12, M11, R2
VCCIO	– *(16)*	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12
GNDINT	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K7,K10, L6, L11, M5, M12, T8	E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K7,K10, L6, L11, M5, M12, T8
GNDIO	–	–	–
No Connect (N.C.)	–	A8, B8, D1, D14, D16, E1, E3, E13, E14, E15, E16, F14, F15, F16, G3, H1, H4, H16, J1, J2, K2, K3, K12, K14, K15, K16, L2, L4, M2, M3, M4, M14, M16, N1, N2, N3, N14, N15, P2, P11, P14 *(7)*	–
Total User I/O Pins *(8)*	189	150	191

Table 120. FLEX 10K Device Pin-Outs (Part 1 of 2)   *Note (1)*

Pin Name	356-Pin BGA EPF10K30 EPF10K30A	356-Pin BGA EPF10K50 EPF10K50V EPF10K100A	403-Pin PGA EPF10K50
MSEL0 *(2)*	D4	D4	AN1
MSEL1 *(2)*	D3	D3	AR1
nSTATUS *(2)*	D24	D24	AU37
nCONFIG *(2)*	D2	D2	AU1
DCLK *(2)*	AC5	AC5	E1
CONF_DONE *(2)*	AC24	AC24	C37
INIT_DONE *(3)*	T24	T24	R35
nCE *(2)*	AC2	AC2	G1
nCEO *(2)*	AC22	AC22	E37
nWS *(4)*	AE24	AE24	E31
nRS *(4)*	AE23	AE23	A33
nCS *(4)*	AD24	AD24	A35
CS *(4)*	AD23	AD23	C33
RDYnBSY *(4)*	U22	U22	N35
CLKUSR *(4)*	AA24	AA24	G35
DATA7 *(4)*	AF4	AF4	C9
DATA6 *(4)*	AD8	AD8	A7
DATA5 *(4)*	AE5	AE5	E9
DATA4 *(4)*	AD6	AD6	C7
DATA3 *(4)*	AF2	AF2	A5
DATA2 *(4)*	AD5	AD5	E7
DATA1 *(4)*	AD4	AD4	C5
DATA0 *(2)*, *(5)*	AD3	AD3	C1
TDI *(2)*	AC3	AC3	J1
TDO *(2)*	AC23	AC23	G37
TCK *(2)*	AD25	AD25	A37
TMS *(2)*	D22	D22	AN37
TRST *(2)*	D23	D23	AR37
Dedicated Inputs	A13, B14, AF14, AE13,	A13, B14, AF14, AE13	A17, A21, AU17, AU21
Dedicated Clock Pins	A14, AF13	A14, AF13	A19, AU19
DEV_CLRn *(3)*	AD13	AD13	C17
DEV_OE *(3)*	AE14	AE14	C19

Table 120. FLEX 10K Device Pin-Outs (Part 2 of 2)   *Note (1)*

Pin Name	356-Pin BGA EPF10K30 EPF10K30A	356-Pin BGA EPF10K50 EPF10K50V EPF10K100A	403-Pin PGA EPF10K50
VCCINT	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	B2, D14, E25, F22, K36, T2, T32, V6, AD34, AE5, AL5, AM6, AM20, AN25, AN29, AP4, AT16, AT36
VCCIO	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	B22, D34, E11, E27, F16, L5, L33, P4, T6, T36, V32, AB36, AG5, AG33, AH2, AM18, AM32, AN11, AN27, AP24, AT22
GNDINT	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	B16, B36, D4, E21, F18, F32, G33, P34, U5, Y32, AA33, AB2, AB6, AH36, AM16, AN17, AN21, AP14, AT2
GNDIO	–	–	B10, B28, D24, E5, E19, E33, F6, F20, K2, W5, W33, Y6, AB32, AD4, AM22, AN5, AN19, AN33, AP34, AT10, AT28
No Connect (N.C.)	C1, D1, D26, E1, E2, G1, G5, G23, G26, H1, H25, H26, J25, K25, P24, R24, T23, U25, V1, V3, V4, V26, W2, W3, Y1, Y2, Y23, AC26 *(9)*	–	–
Total User I/O Pins *(8)*	246	274	310

Table 121. FLEX 10K Pin-Outs (Part 1 of 3)   *Note (1)*

Pin Name	484-Pin FineLine BGA EPF10K30A	484-Pin FineLine BGA EPF10K50V	484-Pin FineLine BGA EPF10K100A	503-Pin PGA EPF10K70
MSEL0 *(2)*	U4	U4	U4	AT40
MSEL1 *(2)*	V4	V4	V4	AV40
nSTATUS *(2)*	W19	W19	W19	AY4
nCONFIG *(2)*	T7	T7	T7	AY40
DCLK *(2)*	E5	E5	E5	H40
CONF_DONE *(2)*	F18	F18	F18	F4
INIT_DONE *(3)*	K19	K19	K19	V6
nCE *(2)*	E4	E4	E4	K40
nCEO *(2)*	E19	E19	E19	H4
nWS *(4)*	E17	E17	E17	A3
nRS *(4)*	F17	F17	F17	C5
nCS *(4)*	D19	D19	D19	C1
CS *(4)*	D18	D18	D18	C3
RDYnBSY *(4)*	K17	K17	K17	T6
CLKUSR *(4)*	G18	G18	G18	H6
DATA7 *(4)*	E8	E8	E8	E29
DATA6 *(4)*	G7	G7	G7	D30
DATA5 *(4)*	D7	D7	D7	C31
DATA4 *(4)*	E7	E7	E7	B32
DATA3 *(4)*	F6	F6	F6	D32
DATA2 *(4)*	D5	D5	D5	B34
DATA1 *(4)*	E6	E6	E6	E33
DATA0 *(2)*, *(5)*	D4	D4	D4	F40
TDI *(2)*	F5	F5	F5	M40
TDO *(2)*	F19	F19	F19	K4
TCK *(2)*	E18	E18	E18	D4
TMS *(2)*	U18	U18	U18	AT4
TRST *(2)*	V19	V19	V19	AV4
Dedicated Inputs	E12, H11, R12, V11	E12, H11, R12, V11	E12, H11, R12, V11	D20, D24, AY24, AY20
Dedicated Clock Pins	D12, P11	D12, P11	D12, P11	D22, AY22
DEV_CLRn *(3)*	G11	G11	G11	F22
DEV_OE *(3)*	F12	F12	F12	G21

Table 121. FLEX 10K Pin-Outs (Part 2 of 3)   *Note (1)*

Pin Name	484-Pin FineLine BGA EPF10K30A	484-Pin FineLine BGA EPF10K50V	484-Pin FineLine BGA EPF10K100A	503-Pin PGA EPF10K70
VCCINT	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17, BA19
VCCIO	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37
GNDINT	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13, BA25
GNDIO	–	–	–	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W41, W3, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA21, BA23

Table 121. FLEX 10K Pin-Outs (Part 3 of 3)	*Note (1)*		
Pin Name	**484-Pin FineLine BGA EPF10K30A**	**484-Pin FineLine BGA EPF10K50V**	**484-Pin FineLine BGA EPF10K100A**	**503-Pin PGA EPF10K70**
No Connect (N.C.)	A2, A3, A4, A5, A7, A9, A11, A12, A14, A15, A20, A21, B3, B4, B9, B10, B12, B16, B19, B20, C1, C6, C9, C10, C12, C13, C14, C16, C17, C22, D1, D2, D3, D20, D21, E2, E3, E20, E22, F1, F2, F3, F20, F21, G2, G20, G22, H3, J1, J2, J3, J21, J22, K2, K22, L1, L2, L3, L20, L21, L22, M2, M3, M21, M22, N1, N2, N21, N22, P2, P3, P20, P21, P22, R2, R3, R20, R21, T2, T20, T21, U1, U2, U3, U20, U21, U22, V2, V20, W1, W2, W22, Y4, Y9, Y12, Y13, Y16, Y19, Y20, AA2, AA3, AA4, AA9, AA11, AA13, AA15, AA21, AB1, AB2, AB3, AB4, AB5, AB7, AB8, AB9, AB12, AB15, AB17, AB18, AB19, AB20, AB21, AB22 *(9)*	A2, A3, A4, A5, A7, A9, A11, A12, A14, A15, A20, A21, B3, B4, B9, B10, B12, B16, B19, B20, C1, C6, C9, C10, C12, C13, C14, C16, C17, D1, D2, D3, D20, E20, F2, J2, K2, L2, N1, P20, P22, R3, T20, T21, U1, U3, W22, Y4, Y9, Y12, Y13, Y16, Y19, Y20, AA2, AA3, AA4, AA9, AA11, AA13, AA15, AA21, AB1, AB2, AB3, AB4, AB5, AB7, AB8, AB9, AB12, AB15, AB17, AB18, AB19, AB20, AB21, AB22 *(10)*	–	A19, A21, A23, A31, A33, A35, A39, A41, B16, B18, B22, B24, B30, B40, C29, C35, D18, D26, D28, D38, E27, E37, F18, F2, F26, F30, F32, G23, G25, G29, G31, G33, G35, K6, K42, L39, L43, M2, N7, P38, P4, P42, R37, T40, V42, AC5, AD2, AE3 *(11)*
Total User I/O Pins *(8)*	246	291	369	358

Table 122. FLEX 10K Pin-Outs (Part 1 of 3)   *Note (1)*

Pin Name	503-Pin PGA EPF10K100	599-Pin PGA EPF10K130V EPF10K250A	600-Pin BGA EPF10K100A	600-Pin BGA EPF10K130V EPF10K250A
MSEL0 (2)	AT40	F6	F5	F5
MSEL1 (2)	AV40	C3	C1	C1
nSTATUS (2)	AY4	E43	D32	D32
nCONFIG (2)	AY40	B4	D4	D4
DCLK (2)	H40	BE5	AP1	AP1
CONF_DONE (2)	F4	BC43	AM32	AM32
INIT_DONE (3)	V6	AM40	AE32	AE32
nCE (2)	K40	BB6	AN2	AN2
nCEO (2)	H4	BF44	AP35	AP35
nWS (4)	A3	BB40	AR29	AR29
nRS (4)	C5	BA37	AM28	AM28
nCS (4)	C1	AY38	AL29	AL29
CS (4)	C3	BA39	AN29	AN29
RDYnBSY (4)	T6	AW47	AG35	AG35
CLKUSR (4)	H6	AY42	AM34	AM34
DATA7 (4)	E29	BD14	AM13	AM13
DATA6 (4)	D30	BA17	AR12	AR12
DATA5 (4)	C31	BB16	AN12	AN12
DATA4 (4)	B32	BF12	AP11	AP11
DATA3 (4)	D32	BG11	AM11	AM11
DATA2 (4)	B34	BG9	AR10	AR10
DATA1 (4)	E33	BF10	AN10	AN10
DATA0 (2), (5)	F40	BC5	AM4	AM4
TDI (2)	M40	BF4	AN1	AN1
TDO (2)	K4	BB42	AN34	AN34
TCK (2)	D4	BE43	AL31	AL31
TMS (2)	AT4	F42	C35	C35
TRST (2)	AV4	B46	C34	C34
Dedicated Inputs	D20, D24, AY24, AY20	B24, C25, BG25, BG23	C18, D18, AM18, AN18	C18, D18, AM18, AN18
Dedicated Clock Pins	D22, AY22	BF24, A25	AL18, E18	AL18, E18
LOCK (12)	AV14	–	–	–
GCLK1 (13)	AY22	–	–	–
DEV_CLRn (3)	F22	BE23	AR17	AR17

Table 122. FLEX 10K Pin-Outs (Part 2 of 3) *Note (1)*				
Pin Name	**503-Pin PGA EPF10K100**	**599-Pin PGA EPF10K130V EPF10K250A**	**600-Pin BGA EPF10K100A**	**600-Pin BGA EPF10K130V EPF10K250A**
DEV_OE *(3)*	G21	BC25	AR19	AR19
VCCINT	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17	A3, A45, C1, C11, C19, C29, C37, C47, E5, G25, L3, L45, W3, W45, AJ3, AJ45, AU3, AU45, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45	A11, A19, B1, B18, D24, E2, F31, F35, H1, K32, M2, N34, P5, T35, U3, V32, Y2, AA33, AB5, AD35, AE4, AF32, AG5, AK31, AK35, AL3, AP24, AR11, AR18	A11, A19, B1, B18, D24, E2, F31, F35, H1, K32, M2, N34, P5, T35, U3, V32, Y2, AA33, AB5, AD35, AE4, AF32, AG5, AK31, AK35, AL3, AP24, AR11, AR18
VCCIO	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37	D24, E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AD4, AD44, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39, BD24	A20, A27, C2, C3, C4, C8, C15, C23, C32, C33, D5, D31, E5, E12, E31, AL5, AL12, AM5, AM19, AM26, AM31, AN3, AN4, AN8, AN15, AN32, AN33, AP34, AR23	A20, A27, C2, C3, C4, C8, C15, C23, C32, C33, D5, D31, E5, E12, E31, AL5, AL12, AM5, AM19, AM26, AM31, AN3, AN4, AN8, AN15, AN32, AN33, AP34, AR23
VCC_CKLK *(14)*	BA19	–	–	–
GNDINT	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13	A47, B2, C13, C21, C27, C35, C45, D4, G23, N3, N45, AA3, AA45, AG3, AG45, AR3, AR45, BD44, BE3, BE13, BE21, BE27, BE35, BE45, BG1, BG47	A1, A2, A3, A4, A5, A18, A31, A32, A33, A34, A35, B2, B3, B4, B5, B6, B31, B32, B33, B34, B35, C5, C6, C30, C31, D6, D30, E6, AN35	A1, A2, A3, A4, A5, A18, A31, A32, A33, A34, A35, B2, B3, B4, B5, B6, B31, B32, B33, B34, B35, C5, C6, C30, C31, D6, D30, E6, AN35
GNDIO	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W3, W41, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA23, BA21	E7, E13, E19, E29, E35, E41, F24, G5, G43, H40, N5, N43, W5, W43, AD6, AD42, AJ5, AJ43, AR5, AR43, AY8, AY40, BA5, BA43, BB24, BC7, BC13, BC19, BC29, BC35, BC41	E30, AL6, AL30, AM6, AM30, AN5, AN6, AN30, AN31, AP2, AP3, AP4, AP5, AP6, AP30, AP31, AP32, AP33, AR1, AR2, AR3, AR4, AR5, AR30, AR31, AR32, AR33, AR34, AR35	E30, AL6, AL30, AM6, AM30, AN5, AN6, AN30, AN31, AP2, AP3, AP4, AP5, AP6, AP30, AP31, AP32, AP33, AR1, AR2, AR3, AR4, AR5, AR30, AR31, AR32, AR33, AR34, AR35
GND_CKLK *(14)*	BA25	–	–	–

Table 122. FLEX 10K Pin-Outs (Part 3 of 3)   *Note (1)*

Pin Name	503-Pin PGA EPF10K100	599-Pin PGA EPF10K130V EPF10K250A	600-Pin BGA EPF10K100A	600-Pin BGA EPF10K130V EPF10K250A
No Connect (N.C.)	–	–	D1, D2, D3, E1, E3, E4, E32, F1, F2, F3, F4, G1, G2, G3, G4, G5, H5, D33, D34, D35, E33, E34, E35, F32, F33, F34, G31, G32, G33, G34, G35, H31, AB31, AB32, AB33, AB34, AC31, AC32, AC33, AC34, AC35, AD31, AD32, AD33, AD34, AE33, AE34, AE35, AH5, AJ2, AJ3, AJ4, AJ5, AK1, AK2, AK3, AK4, AK5, AL1, AL2, AL4, AM1, AM2, AM3 *(15)*	–
Total User I/O Pins *(8)*	406	470	406	470

Notes to tables:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin `TRST` is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, `LOCK` is driven high. `LOCK` remains high if a periodic clock stops clocking. The `LOCK` function is optional; if the `LOCK` output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no V_{CCIO} pins.

Revision History

The information contained in the *FLEX 10K Embedded Programmable Logic Family Data Sheet* version 4.02 supersedes information published in previous versions.

Version 4.02

The following changes were made to the *FLEX 10K Embedded Programmable Logic Family Data Sheet* version 4.02:

- Added additional text to Note (2) on page 51.
- Added Note (1) to Figure 13 on page 29.
- Added Note (1) to Table 12 on page 39.
- Added Note (16) to Table 119 on page 128.
- Updated Figure 26 on page 56.

Version 4.01

The following changes were made to the *FLEX 10K Embedded Programmable Logic Family Data Sheet* version 4.01:

- Updated information on the chip-wide output enable and chip-wide reset pins in the I/O Element section on page 32.
- Updated Note (2) on page 45.