

Designing for Migration to Actel MPGAs

The Actel Mask Programmed Gate Array (MPGA) family of high-density, high-performance devices comprises mask programmed versions of the ACT 1, ACT 2, 1200XL, 3200DX, and ACT 3/ACT 3 PCI Field Programmable Gate Array (FPGA) families. The MPGA family provides a low-risk conversion path from programmable gate arrays to production quantity devices. By significantly reducing the production costs of a product without technical or time-to-market risks, MPGAs prolong the life cycle of a finished design.

The MPGA products are specifically designed to make conversion from programmable devices virtually transparent to all members of a product team, from initial system designers to final production manufacturing personnel. Virtually any successful FPGA design can be successfully converted to an MPGA device without difficulty. Figure 9 shows the design process for Actel FPGA and MPGA devices. The design flow is tailored to ensure that the conversion process is as seamless as possible, but adhering to some simple guidelines will further ease the transformation. Use the following suggestions and design hints during the FPGA development process to make each design as convertible as possible.

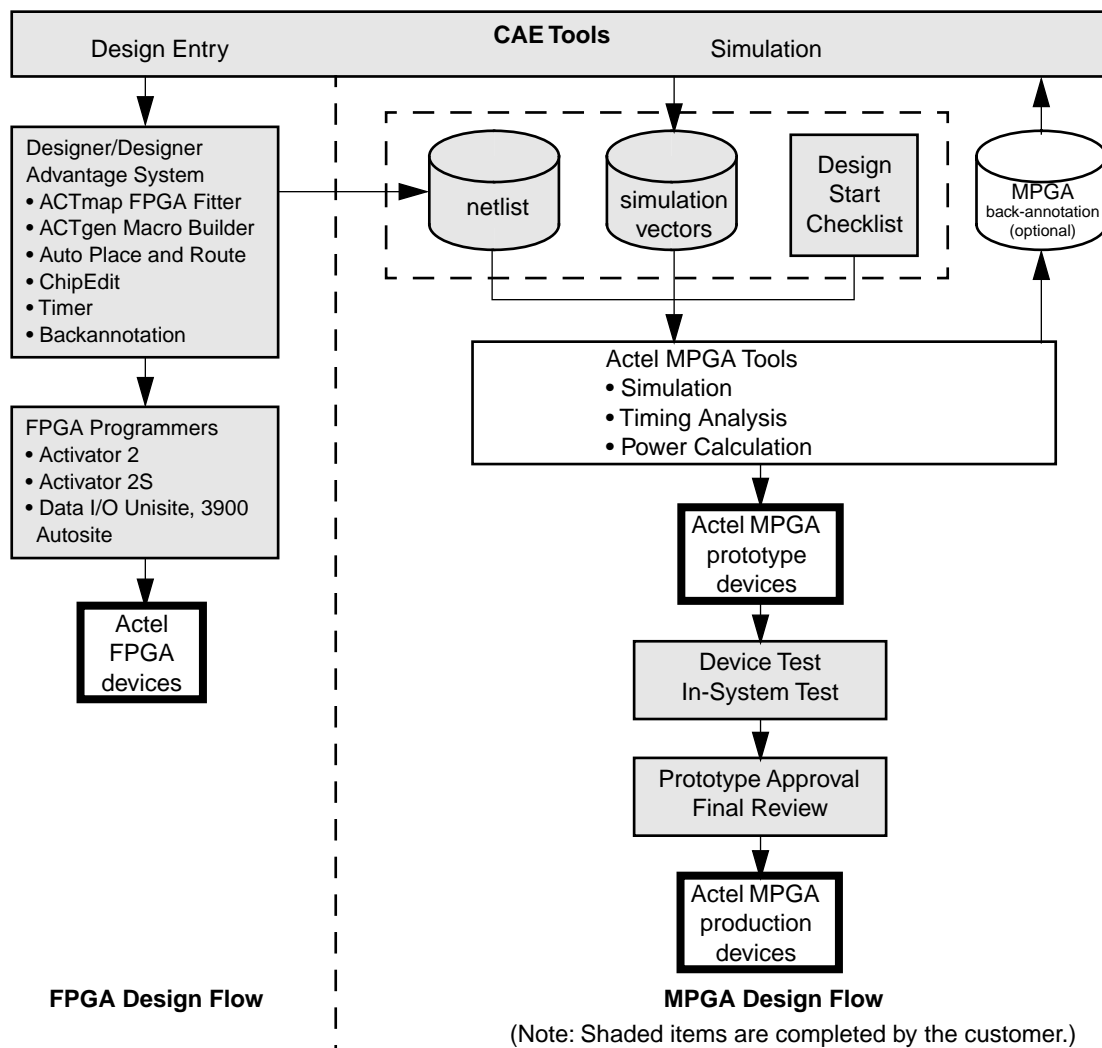


Figure 9 • Actel Device Design Flow

General Design Guidelines

Fundamental principles should be applied to all digital designs regardless of the intended target devices. Actel FPGA designs and their corresponding MPGA versions are no different; reliable systems result from solid circuit designs. Design practices such as reducing unnecessary logic (for example, inverters) using DeMorgan's Law to combine logic, and balancing logic levels (and their corresponding delays) between registers will all help to produce stable circuits. The *Actel FPGA Data Book and Design Guide* includes many application notes to assist in the design process.

MPGA versus FPGA Performance

Actel MPGAs are built using a “sea-of-gates” architecture. This architecture is similar to the FPGA architecture but has more compact spacing between logic modules and tighter metal-only interconnections. It enables MPGAs to provide performance equal or superior to their FPGA counterparts for almost every design. On average, both logic module and routing speeds are significantly faster for MPGAs. This usually translates into superior system performance for the same design.

Some designs that use ACT 3 devices to satisfy very high on-chip and off-chip performance requirements may experience a small decrease in speed. The ACT 3 I/O modules are especially fast and are not implemented identically in the MPGA versions. However, in most cases, the MPGA is still fast enough as a drop-in replacement for any Actel FPGA. Check the MPGA data sheet to verify that its I/O performance satisfies your particular system requirement. MPGA migration is also available for ACT 3 PCI products.

Power

Due to its relatively smaller die size and metal-only interconnections, MPGA power dissipation is usually significantly lower than its FPGA counterpart. The active power dissipation of a CMOS device is a function of its equivalent capacitance. On average, the removal of programmable elements from the device reduces its equivalent capacitance and, in turn, its active power dissipation. Upon receipt of the Design Start Checklist and associated materials, Actel calculates the MPGA active power dissipation for each design based on this formula. This calculation is immediately relayed to you so that you can update system power specifications accordingly.

Use Synchronous Design

Asynchronous designs are often the cause of many problems, especially when a change is made among target devices to implement a design. An asynchronous design that works with SSI/MSI devices may translate poorly to other technologies such as ASICs because of significant differences in timing

between devices. Designs using the same technology from a single manufacturer still may fail because of process differences from die to die. Even similar devices such as Actel FPGAs and MPGAs may not automatically implement an asynchronous design without problems. Generally, most of the problems come from small timing differences that lead to functional errors and days of debugging.

Synchronous design significantly increases the reliability of a circuit. It also makes systems easier to test and debug. The odds of successfully migrating to Actel MPGAs increase directly with the elimination of asynchronous elements in the design. In particular, try to avoid the following types of potential problem circuits:

1. **glitch generators**—Avoid circuits that may create pulses or glitches whose widths depend on variations in propagation delay. For example, an asynchronously generated clock signal generated by decoding the output of a counter with combinatorial logic may work in one technology but may fail to generate a proper rising edge in another. The same decoder may create extra, unwanted clock pulses if the decoder has uneven levels of logic from input to output.
2. **gated clocks**—Do not gate clock inputs to edge triggered storage elements. Use flip-flops with enable inputs instead. Not only is this more reliable, but it also saves logic resources.
3. **asynchronously generated reset signals**—Flip-flops or latches implemented to create asynchronous one-shot signals are unreliable and untestable. Whenever the output of a storage element is fed back to its asynchronous input, the resulting pulse varies widely in behavior depending on process and environmental variations.
4. **internal delay lines**—Strings of buffers or inverters used to create ring oscillators or internal delay lines have unpredictable delay and frequency. They are also extremely difficult to test. Use stable, external oscillators and synchronous pulse generators as alternatives.

Sometimes asynchronous elements must be included in a design. In that case, be sure to understand the effects that technology, process, and environmental variations have on each circuit. Refer to industry standard ASIC logic design manuals for more complete information about creating reliable, testable designs.

Testability

Actel FPGAs are fully testable after programming using two Silicon Explorer circuits built into every device. Any node may be observed in-circuit, in real time to determine its behavior under any stimulus. The Silicon Explorer helps to verify the results of static timing analysis along with

functional and backannotated simulation. Actel MPGAs do not include Silicon Explorer circuits, so it is important to design testable circuits into the FPGA from the beginning before converting to an MPGA. A complete simulation procedure for thorough testing is essential to ensure the success of FPGA and MPGA designs. Make sure that the simulation procedures test each section of the chip thoroughly for proper functionality under a wide variety of inputs.

Some common methods to make each design more testable include the following:

- Add global reset inputs to all sequential logic.
- Use global, minimal skew clock signals.
- Use unused I/O pins to observe important internal nodes.
- Use loadable synchronous counters.
- Remove asynchronous logic loops.
- Remove asynchronous one-shot pulse generators.

[Use ACTgen Macro Builder or Actel Soft Macro Library](#)

The Actel Designer and Designer Advantage systems include ACTgen Macro Builder software to create fast, reliable soft macros automatically. You can use ACTgen to generate customized macros such as counters, registers, decoders, adders, and multiplexers according to precise specifications. For other types of high-level functions, use the Actel soft macro libraries. Whether coming from ACTgen or the Actel libraries, Actel soft macros are easily migrated from FPGA to MPGA devices because of their built-in reliability and testability.

[I/O Pin Assignment](#)

The performance and routability of Actel FPGA designs are largely determined by the effectiveness of the I/O pin assignments. Likewise, corresponding MPGA conversions have an equally important dependence upon pin placements. Actel's Designer and Designer Advantage development systems include I/O placement software to determine automatically excellent locations for the I/Os, depending on circuit topology and device resources. Since automatic pin placement generally produces superior results versus a design with manual placements, it is important to limit the number of manually placed pin locations as much as possible.

Since MPGA devices are specifically designed to be drop-in replacements for FPGAs, there is no need to change the I/O pin assignments as part of the conversion process. If at all possible, it is best to retain an identical pinout for all versions of a design. The performance of the MPGA may be adversely affected if many changes are made to the pin placements. However, Actel will modify the MPGA pin placements if any changes are necessary.

[Summary](#)

By following these design hints and guidelines, the conversion from programmable devices is virtually transparent to all members of a product team. Virtually any successful FPGA design can be replaced by a drop-in replacement without difficulty.

