**Timing of digital gates**

Digital gates are electronic components and as such have capacitance and resistances that delay the signal through them. Consider the inverter in the figure below any input signal is inverted at the output but also changed in shape and delayed

 In Out

Consider the waveform shown below, the input signal and the output signal each have different slopes and delayed.



The propagation delays ,  and the rise time or fall time . The latter parameters are defined respectively below:

* **tr**is the rise time of the output signal between %10 and %90 levels.
* **tf** is the fall time of the output signal between %10 and %90 levels.
* **tPHL**is the propagation delay high to low at %50 levels of the rise time of the input and %50 level of the output.
* **tPLH**is the propagation delay low to high at %50 levels of the rise time of the input and %50 level of the output.

To simplify the calculation of delay, we assume that Delay, d of a gate is given as

 d = ( **t**PHL + **t**PLH) / 2

When this is approximated for **tr**=0 and **tf**=0 then the equation becomes simpler. This is shown

below, where only delay of the in/out signals are considered.

in

out

Delay, d

The behaviour of the circuits is different when we consider delay time and when we ignore it. In many cases if the timing is not taken into account incorrect results are obtained. This is particularly true for sequential circuits. The example below shows the effect of the timing.

**Example**

Draw the **timing diagram** for F(a,b) = b’ ⊕ a for the following consecutive vector inputs:

 ab= 00, 10, 01, 11 (\*\*follow these vectors in order given. Start from AB=00 \*\*). Assume the following gate delays, INV.= 2ns , XOR gate = 5ns.

**2ns** delay

**5ns** delay

**a**

**b**

F

**Timing without Delay**

**a) Start by calculating the critical path.**

**b) Draw timing scales for each vector in accordance with the critical path timing (Vertical lines).**

**c) Draw Variable lines for each variable and any compound variable (horizontal lines).**

**d) Follow Vectors in order given and draw timing edges.**

**e) Calculate each variable variation and draw the edges corresponding to the change in variables.**

**For Zero gates delay the diagram below is drawn. Follow the changes in input at any instant and the edges of the signals and see the final function F waveform.**

ab=00 ab=10 ab=01 ab=11

b

a

b’

F

10ns 10ns 10ns 10ns



Total delay is 7 ns => take period of 10 ns.

Now consider the circuit again and introduce the timing of the gates. First we calculate the critical path, in this case is 2+5=7 ns, therefor we will consider 50 ns timing analysis in interval of greater than 7. Let us use 10 ns. So each input vector is applied for 10 ns and the waveform changes through the gates is followed as shown below.



Edges that cause change in the output are shown with an arrow after delay of going through the gate.