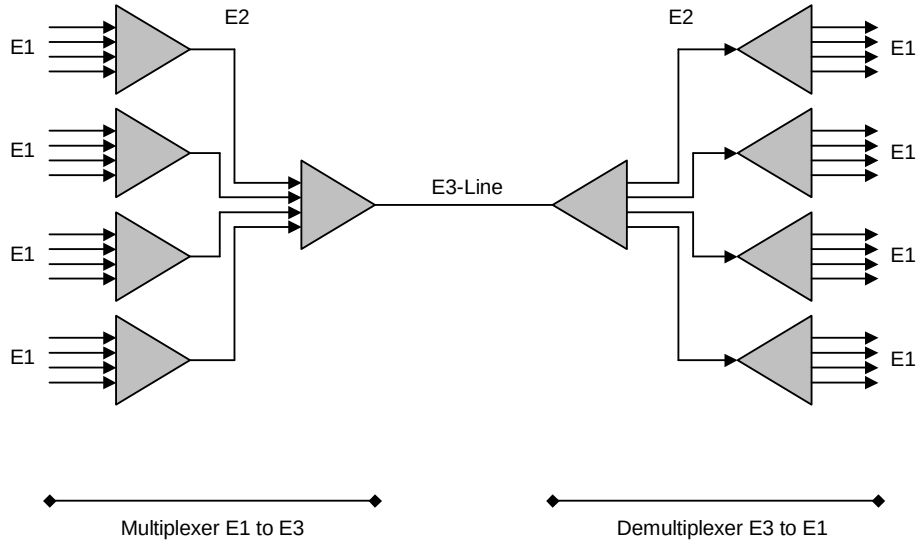
Multiplexer / Demultiplexer : E1 to / from E3 according ITU-T G.703 / G.742 / G.751

For transmitting many E1 channels over one line, the ITU describes in the standard G.742 a method for multiplexing four E1 channels to one E2 channel and in the standard G.751 a method for multiplexing four E2 channels to one E3 channel. The used technique is Time Division Multiplexing (TDM).

This document describes the two modules which incorporates the multiplexing and demultiplexing function needed for transmitting 16 E1 channels transparent over one E3 channel.

The multiplexing/demultiplexing is done in two stages :

- First from E1 to E2
- Second from E2 to E3



Acronym	E1	E2	E3
Standard	ITU-T G.703	ITU-T G.703	ITU-T G.703
Datarate	2048 kbit/sec	8448 kbit/sec	34368 kbit/sec
Tolerance	50 ppM	30 ppM	20 ppM

Acronym	Multiplexing E1 to E2	Multiplexing E2 to E3
Standard	ITU-T G.742	ITU-T G.751

The design is written in VHDL. It's plain VHDL, the single special component is a Xilinx® 16-bit CLB-RAMs (RAM16X1D) which is used for FIFOs. The design could be easy translated to an Altera® or Lattice® device.

Features

The sixteen E1 input interfaces can be used fully asynchronous compared to the E3 reference clock and the other E1 input clocks. The individual clock enable input for any E1 input interface enables the possibility of working with a higher interface clock rate (like 34.368 MHz). The whole clock-system can be sourced with only one clock too. This is often useful in a greater system.

The Remote Alarm Indication (RAI) and the National Bit (Na) of the E3 frame and the four incorporated E2 frames can be used fully independent of each other.

The generation of the internally needed E2 clock (8448 kHz) is done internally by a special division stage from the E3 reference clock (34.368 MHz).

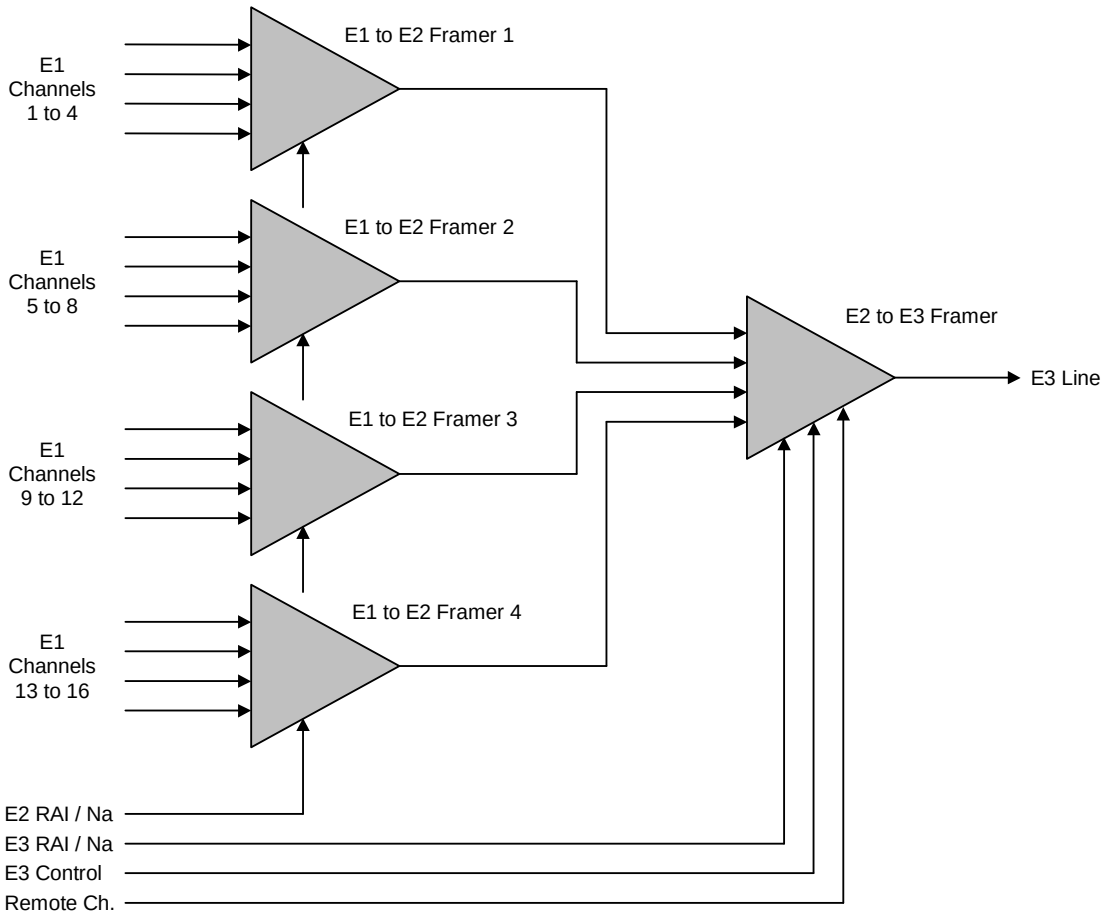
It's possible to transmit idle-0 or idle-1 in the E3 payload.
It's also possible to transmit an unframed 0 or 1 level.

For testing purposes it's possible to transmit defective Frame Alignment Signals (FAS) to check the counterpart deframer.

An extra data channel in the overhead bits of the E3 frame enables the possibility to transmit user or control data with a data rate of nearly 90 kbit/sec. This feature is fully compliant with the ITU standards. In detail it uses the first four justification control bits (C_{J1}, J=1..4) in the E3 frame overhead. This is possible because the receiver performs a majority-decision with the three justification control nibbles (C_{J1},C_{J2},C_{J3}, J=1..4) when deciding if a justification must be done or not. One erroneous nibble doesn't affect the justification decision.

Combined error outputs for the E1 and the E2 domain reports problems with the signal clocking. If a E1 interface clock is too fast or too slow compared with the E3 reference clock, the E1 interface data are delivered too fast or too slow. This causes a FIFO overflow or an underflow. This event is reported on the combined error output.

Multiplexer (simplified)



Multiplexer : VHDL-Entity

```
entity MULTIPLEXER_E1_TO_E3 is
  port (
    E3_REF_CLK      : in  std_logic;                     -- Framer Clock E3
    RESET           : in  std_logic;                     -- Reset
    E2_CH1_RAI      : in  std_logic;                     -- E2 Channel 1 Remote Alarm Indication
    E2_CH1_NA       : in  std_logic;                     -- E2 Channel 1 National Bit
    E2_CH2_RAI      : in  std_logic;                     -- E2 Channel 2 Remote Alarm Indication
    E2_CH2_NA       : in  std_logic;                     -- E2 Channel 2 National Bit
    E2_CH3_RAI      : in  std_logic;                     -- E2 Channel 3 Remote Alarm Indication
    E2_CH3_NA       : in  std_logic;                     -- E2 Channel 3 National Bit
    E2_CH4_RAI      : in  std_logic;                     -- E2 Channel 4 Remote Alarm Indication
    E2_CH4_NA       : in  std_logic;                     -- E2 Channel 4 National Bit
    E3_RAI          : in  std_logic;                     -- E3 Remote Alarm Indication
    E3_NA           : in  std_logic;                     -- E3 National Bit
    E3_FRAME_START  : out std_logic;                     -- E3 Frame Pulse
    E3_IDLE_SET     : in  std_logic;                     -- E3 Pulse : new IDLE Command
    E3_IDLE_CMD     : in  std_logic_vector (2 downto 0); -- E3 IDLE Command
    E3_FAS_SET      : in  std_logic;                     -- E3 Pulse : new FAS Command
    E3_FAS_CMD      : in  std_logic_vector (2 downto 0); -- E3 FAS Command
    E3_REMOTE_EN    : in  std_logic;                     -- E3 Remote Channel : Enable
    E3_REMOTE_DATA  : in  std_logic_vector (3 downto 0); -- E3 Remote Channel : TX Data
    E1_CH11_TX_CLK  : in  std_logic;                     -- E1 Channel 11 Clock
    E1_CH11_TX_VAL  : in  std_logic;                     -- E1 Channel 11 Data Valid
    E1_CH11_TX_DATA : in  std_logic;                     -- E1 Channel 11 Data
    E1_CH12_TX_CLK  : in  std_logic;                     -- E1 Channel 12 Clock
    E1_CH12_TX_VAL  : in  std_logic;                     -- E1 Channel 12 Data Valid
    E1_CH12_TX_DATA : in  std_logic;                     -- E1 Channel 12 Data
    E1_CH13_TX_CLK  : in  std_logic;                     -- E1 Channel 13 Clock
    E1_CH13_TX_VAL  : in  std_logic;                     -- E1 Channel 13 Data Valid
    E1_CH13_TX_DATA : in  std_logic;                     -- E1 Channel 13 Data
    E1_CH14_TX_CLK  : in  std_logic;                     -- E1 Channel 14 Clock
    E1_CH14_TX_VAL  : in  std_logic;                     -- E1 Channel 14 Data Valid
    E1_CH14_TX_DATA : in  std_logic;                     -- E1 Channel 14 Data
    E1_CH21_TX_CLK  : in  std_logic;                     -- E1 Channel 21 Clock
    E1_CH21_TX_VAL  : in  std_logic;                     -- E1 Channel 21 Data Valid
    E1_CH21_TX_DATA : in  std_logic;                     -- E1 Channel 21 Data
    E1_CH22_TX_CLK  : in  std_logic;                     -- E1 Channel 22 Clock
    E1_CH22_TX_VAL  : in  std_logic;                     -- E1 Channel 22 Data Valid
    E1_CH22_TX_DATA : in  std_logic;                     -- E1 Channel 22 Data
    E1_CH23_TX_CLK  : in  std_logic;                     -- E1 Channel 23 Clock
    E1_CH23_TX_VAL  : in  std_logic;                     -- E1 Channel 23 Data Valid
    E1_CH23_TX_DATA : in  std_logic;                     -- E1 Channel 23 Data
    E1_CH24_TX_CLK  : in  std_logic;                     -- E1 Channel 24 Clock
    E1_CH24_TX_VAL  : in  std_logic;                     -- E1 Channel 24 Data Valid
    E1_CH24_TX_DATA : in  std_logic;                     -- E1 Channel 24 Data
    E1_CH31_TX_CLK  : in  std_logic;                     -- E1 Channel 31 Clock
    E1_CH31_TX_VAL  : in  std_logic;                     -- E1 Channel 31 Data Valid
    E1_CH31_TX_DATA : in  std_logic;                     -- E1 Channel 31 Data
    E1_CH32_TX_CLK  : in  std_logic;                     -- E1 Channel 32 Clock
    E1_CH32_TX_VAL  : in  std_logic;                     -- E1 Channel 32 Data Valid
    E1_CH32_TX_DATA : in  std_logic;                     -- E1 Channel 32 Data
    E1_CH33_TX_CLK  : in  std_logic;                     -- E1 Channel 33 Clock
    E1_CH33_TX_VAL  : in  std_logic;                     -- E1 Channel 33 Data Valid
    E1_CH33_TX_DATA : in  std_logic;                     -- E1 Channel 33 Data
    E1_CH34_TX_CLK  : in  std_logic;                     -- E1 Channel 34 Clock
    E1_CH34_TX_VAL  : in  std_logic;                     -- E1 Channel 34 Data Valid
    E1_CH34_TX_DATA : in  std_logic;                     -- E1 Channel 34 Data
    E1_CH41_TX_CLK  : in  std_logic;                     -- E1 Channel 41 Clock
    E1_CH41_TX_VAL  : in  std_logic;                     -- E1 Channel 41 Data Valid
    E1_CH41_TX_DATA : in  std_logic;                     -- E1 Channel 41 Data
    E1_CH42_TX_CLK  : in  std_logic;                     -- E1 Channel 42 Clock
    E1_CH42_TX_VAL  : in  std_logic;                     -- E1 Channel 42 Data Valid
    E1_CH42_TX_DATA : in  std_logic;                     -- E1 Channel 42 Data
    E1_CH43_TX_CLK  : in  std_logic;                     -- E1 Channel 43 Clock
    E1_CH43_TX_VAL  : in  std_logic;                     -- E1 Channel 43 Data Valid
    E1_CH43_TX_DATA : in  std_logic;                     -- E1 Channel 43 Data
    E1_CH44_TX_CLK  : in  std_logic;                     -- E1 Channel 44 Clock
    E1_CH44_TX_VAL  : in  std_logic;                     -- E1 Channel 44 Data Valid
    E1_CH44_TX_DATA : in  std_logic;                     -- E1 Channel 44 Data
    E2_TX_ERR       : out std_logic;                     -- E2 Fifo Error
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```
    E1_TX_ERR       : out std_logic;                    -- E1 Fifo Error
    E3_TX_CLK       : out std_logic;                    -- E3 Output Clock
    E3_TX_DATA      : out std_logic                     -- E3 Output Data
  );
end MULTIPLEXER_E1_TO_E3;
```

Multiplexer : Interface Description

E3_REF_CLK

Base clock for the E3 multiplexer. The whole E3 logic of the framer works with this clock. The E2 clock for the four E2 framer is derived from this clock.

RESET

Asynchronous reset for the whole internal logic (E3, E2 and E1 clock domains) of the multiplexer.

E2_CH1_RAI / E2_CH2_RAI / E2_CH3_RAI / E2_CH4_RAI (E3_REF_CLK synchronous)

Remote Alarm Indication input for the four E2 framer. The bit at this input is sampled at the frame begin (9962.26 times per second) of the corresponding E2 framer. It is transmitted as RAI bit in the E2 frame.

E2_CH1_NA / E2_CH2_NA / E2_CH3_NA / E2_CH4_NA (E3_REF_CLK synchronous)

National Bit input for the four E2 framer. The bit at this input is sampled at the frame begin (9962.26 times per second) of the corresponding E2 framer. It is transmitted as NA bit in the E2 frame.

E3_RAI (E3_REF_CLK synchronous)

Remote Alarm Indication input for the E3 framer. The bit at this input is sampled at the frame begin (22375 times per second) of the E3 framer. It is transmitted as RAI bit in the E3 frame.

E3_NA (E3_REF_CLK synchronous)

National Bit input for the E3 framer. The bit at this input is sampled at the frame begin (22375 times per second) of the E3 framer. It is transmitted as NA bit in the E3 frame.

E3_FRAME_START (E3_REF_CLK synchronous)

This signaling output notifies the begin (first bit) of one frame. It reports this event by a 1 signal for one clock period.

E3_IDLE_SET (E3_REF_CLK synchronous)

Command input. The framer assumes the command word at the E3_IDLE_CMD input with a pulse for one clock period at this input. The execution of the command is done at the next frame begin.

E3_IDLE_CMD (E3_REF_CLK synchronous)

0 0 0 : normal operation, overhead and payload transmission
0 1 0 : transmit ‚0' during frame payload
0 1 1 : transmit ‚1' during frame payload
1 0 0 : transmit idle signal ‚0' (unframed)
1 0 1 : transmit idle signal ‚1' (unframed)

E3_FAS_SET (E3_REF_CLK synchronous)

Command input. The framer assumes the command word at the E2_FAS_CMD input with a pulse for one clock period at this input. The execution of the command is done at the next frame begin.

E3_FAS_CMD (E3_REF_CLK synchronous)

0 0 0 : normal operation
0 1 0 : transmit one defective FAS, only one bit error : 1111000000 instead of 1111010000
0 1 1 : transmit one defective FAS, all bits inverted : 0000101111 instead of 1111010000
1 0 0 : transmit four consecutive FAS, only one bit error : 1111000000 instead of 1111010000
1 0 1 : transmit four consecutive FAS, all bits inverted : 0000101111 instead of 1111010000

E3_REMOTE_EN (E3_REF_CLK synchronous)

Activation input for the data transfer channel to the remote device. Set to 0 if not used.

E3_REMOTE_DATA (E3_REF_CLK synchronous)

Data transfer channel to the remote device. This four bit wide channel is transmitted in the E3 frame overhead instead of the first four justification control bits (C_{J1}). It's possible because the receiver performs a majority-decision with the three justification control nibbles (C_{J1},C_{J2},C_{J3}) when deciding if a justification must be done or not. One erroneous nibble doesn't affect the justification decision.
The transmit rate in this channel is 22375 nibbles per second or 89500 bit/sec. The nibble at this input is sampled at the E3 frame begin.

E1_CH11_TX_CLK / E1_CH12_TX_CLK / E1_CH13_TX_CLK / E1_CH14_TX_CLK /
E1_CH21_TX_CLK / E1_CH22_TX_CLK / E1_CH23_TX_CLK / E1_CH24_TX_CLK /
E1_CH31_TX_CLK / E1_CH32_TX_CLK / E1_CH33_TX_CLK / E1_CH34_TX_CLK /
E1_CH41_TX_CLK / E1_CH42_TX_CLK / E1_CH43_TX_CLK / E1_CH44_TX_CLK

Clock for the sixteen E1 TX interface channels. Could be asynchronously regarding to the other E1 channels and to the E3_REF_CLK. The nominal data rate is 2048 kbit/sec.
The inputs E1_CH1x_TX_CLK are connected to the first E2 multiplexer.
The inputs E1_CH2x_TX_CLK are connected to the second E2 multiplexer.
The inputs E1_CH3x_TX_CLK are connected to the third E2 multiplexer.
The inputs E1_CH4x_TX_CLK are connected to the fourth E2 multiplexer.

E1_CH11_TX_VAL / E1_CH12_TX_VAL / E1_CH13_TX_VAL / E1_CH14_TX_VAL /
E1_CH21_TX_VAL / E1_CH22_TX_VAL / E1_CH23_TX_VAL / E1_CH24_TX_VAL /
E1_CH31_TX_VAL / E1_CH32_TX_VAL / E1_CH33_TX_VAL / E1_CH34_TX_VAL /
E1_CH41_TX_VAL / E1_CH42_TX_VAL / E1_CH43_TX_VAL / E1_CH44_TX_VAL

Clock enable input for the sixteen E1 TX interface channels. Set to 1 when using a 2.048 MHz E1 clock. Used when working with a higher clock (like 34.368 MHz) which is used as a single clock for a greater system. When this input is at 1 during the rising edge on the corresponding channel clock input, the data bit at the corresponding channel data input is registered in the input FIFO.
The inputs E1_CH1x_TX_VAL are connected to the first E2 multiplexer.
The inputs E1_CH2x_TX_VAL are connected to the second E2 multiplexer.
The inputs E1_CH3x_TX_VAL are connected to the third E2 multiplexer.
The inputs E1_CH4x_TX_VAL are connected to the fourth E2 multiplexer.

E1_CH11_TX_DATA / E1_CH12_TX_DATA / E1_CH13_TX_DATA / E1_CH14_TX_DATA / E1_CH21_TX_DATA / E1_CH22_TX_DATA / E1_CH23_TX_DATA / E1_CH24_TX_DATA / E1_CH31_TX_DATA / E1_CH32_TX_DATA / E1_CH33_TX_DATA / E1_CH34_TX_DATA / E1_CH41_TX_DATA / E1_CH42_TX_DATA / E1_CH43_TX_DATA / E1_CH44_TX_DATA

User data input for the sixteen E1 TX interface channel. A data bit is sampled with the rising edge on the corresponding channel clock input.
The inputs E1_CH1x_TX_DATA are connected to the first E2 multiplexer.
The inputs E1_CH2x_TX_DATA are connected to the second E2 multiplexer.
The inputs E1_CH3x_TX_DATA are connected to the third E2 multiplexer.
The inputs E1_CH4x_TX_DATA are connected to the fourth E2 multiplexer.

E2_TX_ERR (E3_REF_CLK synchronous)

Combined error signal output from the four E2 interfaces of the E3 TX framer. If one of the four E2 interface channel FIFOs detects a overflow or underflow this error is reported by a 1 signal for the duration of the error.

E1_TX_ERR (E3_REF_CLK synchronous)

Combined error signal output from the E1 interfaces of the four E2 TX framers. If one of the four E1 interface channel FIFOs of a E2 framer detects a overflow or underflow this error is reported by a 1 signal for the duration of the error.

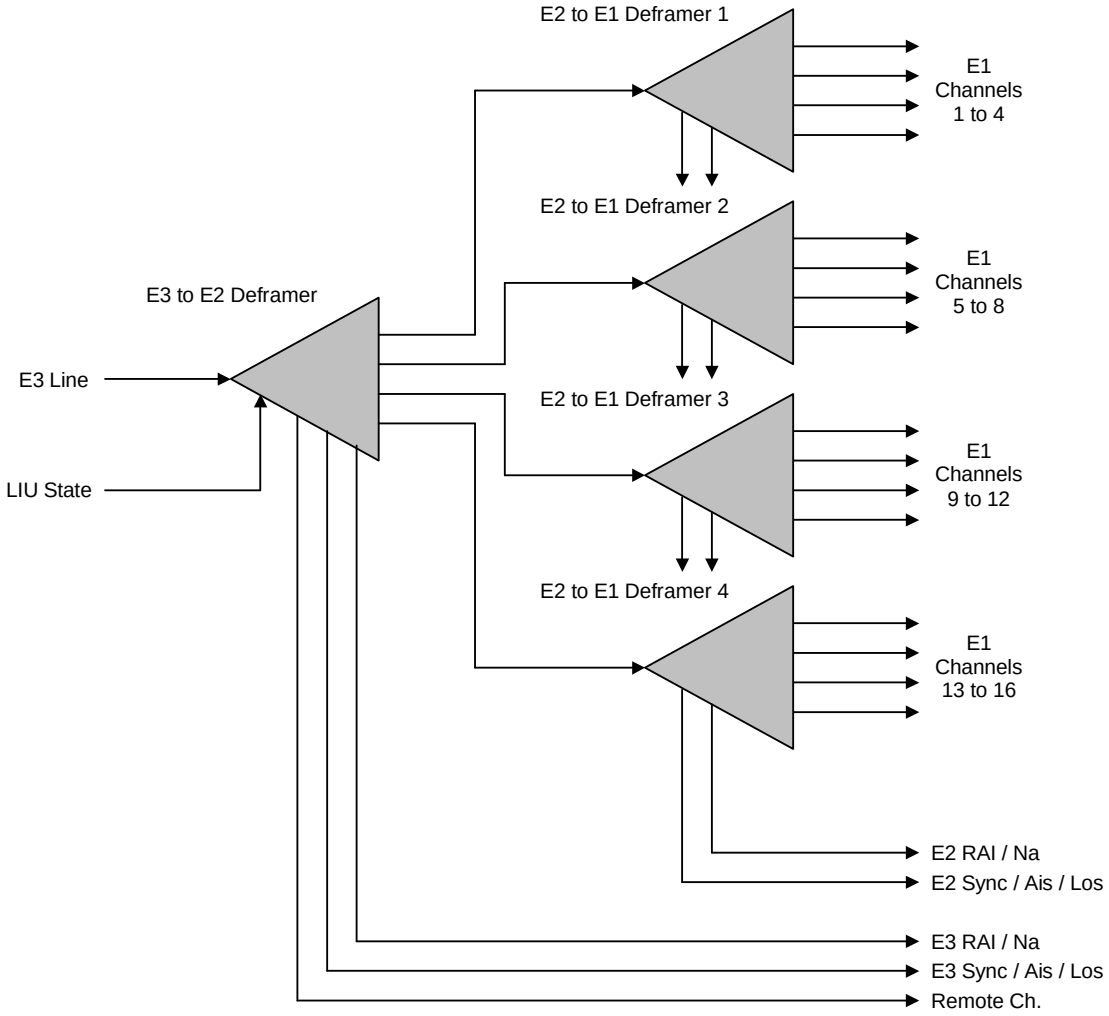
E3_TX_CLK

Output of the E3_REF_CLK to the line interface.

E3_TX_DATA (E3_TX_CLK synchronous)

Serial E3 data output to the line interface.

Demultiplexer (simplified)



Demultiplexer : VHDL-Entity

```
entity DEMULTIPLEXER_E3_TO_E1 is
  port (
    RESET           : in  std_logic;                     -- Reset
    E3_RX_CLK       : in  std_logic;                     -- RX input data clock
    E3_RX_DATA      : in  std_logic;                     -- RX input data signal
    E3_RX_LCV       : in  std_logic;                     -- RX code violation
    E3_RX_LOS       : in  std_logic;                     -- RX loss of signal
    E3_RX_LOL       : in  std_logic;                     -- RX loss of lock
    E3_REF_CLK      : out std_logic;                     -- RX reference clock output
    E3_FRAME_START  : out std_logic;                     -- Frame Pulse
    E3_SYNC         : out std_logic;                     -- State : Frame Synchron
    E3_RAI          : out std_logic;                     -- State : RAI bit
    E3_NA           : out std_logic;                     -- State : NA bit
    E3_AIS          : out std_logic;                     -- State : Alarm Ind. Signal
    E3_LOS          : out std_logic;                     -- State : Loss Of Signal
    E3_REMOTE_EN    : in  std_logic;                     -- Remote Channel : Enable
    E3_REMOTE_DATA  : out std_logic_vector (3 downto 0); -- Remote Channel : RX Data
    E2_CH1_SYNC     : out std_logic;                     -- E2 Channel 1 : Frame Synchronous
    E2_CH1_RAI      : out std_logic;                     -- E2 Channel 1 : RAI Bit
    E2_CH1_NA       : out std_logic;                     -- E2 Channel 1 : NA Bit
    E2_CH1_AIS      : out std_logic;                     -- E2 Channel 1 : Alarm Ind. Signal
    E2_CH1_LOS      : out std_logic;                     -- E2 Channel 1 : Loss Of Signal
    E2_CH2_SYNC     : out std_logic;                     -- E2 Channel 2 : Frame Synchronous
    E2_CH2_RAI      : out std_logic;                     -- E2 Channel 2 : RAI Bit
    E2_CH2_NA       : out std_logic;                     -- E2 Channel 2 : NA Bit
    E2_CH2_AIS      : out std_logic;                     -- E2 Channel 2 : Alarm Ind. Signal
    E2_CH2_LOS      : out std_logic;                     -- E2 Channel 2 : Loss Of Signal
    E2_CH3_SYNC     : out std_logic;                     -- E2 Channel 3 : Frame Synchronous
    E2_CH3_RAI      : out std_logic;                     -- E2 Channel 3 : RAI Bit
    E2_CH3_NA       : out std_logic;                     -- E2 Channel 3 : NA Bit
    E2_CH3_AIS      : out std_logic;                     -- E2 Channel 3 : Alarm Ind. Signal
    E2_CH3_LOS      : out std_logic;                     -- E2 Channel 3 : Loss Of Signal
    E2_CH4_SYNC     : out std_logic;                     -- E2 Channel 4 : Frame Synchronous
    E2_CH4_RAI      : out std_logic;                     -- E2 Channel 4 : RAI Bit
    E2_CH4_NA       : out std_logic;                     -- E2 Channel 4 : NA Bit
    E2_CH4_AIS      : out std_logic;                     -- E2 Channel 4 : Alarm Ind. Signal
    E2_CH4_LOS      : out std_logic;                     -- E2 Channel 4 : Loss Of Signal
    E1_CH11_RX_VAL  : out std_logic;                     -- E1 Channel 11 Data Valid
    E1_CH11_RX_DATA : out std_logic;                     -- E1 Channel 11 Data
    E1_CH12_RX_VAL  : out std_logic;                     -- E1 Channel 12 Data Valid
    E1_CH12_RX_DATA : out std_logic;                     -- E1 Channel 12 Data
    E1_CH13_RX_VAL  : out std_logic;                     -- E1 Channel 13 Data Valid
    E1_CH13_RX_DATA : out std_logic;                     -- E1 Channel 13 Data
    E1_CH14_RX_VAL  : out std_logic;                     -- E1 Channel 14 Data Valid
    E1_CH14_RX_DATA : out std_logic;                     -- E1 Channel 14 Data
    E1_CH21_RX_VAL  : out std_logic;                     -- E1 Channel 21 Data Valid
    E1_CH21_RX_DATA : out std_logic;                     -- E1 Channel 21 Data
    E1_CH22_RX_VAL  : out std_logic;                     -- E1 Channel 22 Data Valid
    E1_CH22_RX_DATA : out std_logic;                     -- E1 Channel 22 Data
    E1_CH23_RX_VAL  : out std_logic;                     -- E1 Channel 23 Data Valid
    E1_CH23_RX_DATA : out std_logic;                     -- E1 Channel 23 Data
    E1_CH24_RX_VAL  : out std_logic;                     -- E1 Channel 24 Data Valid
    E1_CH24_RX_DATA : out std_logic;                     -- E1 Channel 24 Data
    E1_CH31_RX_VAL  : out std_logic;                     -- E1 Channel 31 Data Valid
    E1_CH31_RX_DATA : out std_logic;                     -- E1 Channel 31 Data
    E1_CH32_RX_VAL  : out std_logic;                     -- E1 Channel 32 Data Valid
    E1_CH32_RX_DATA : out std_logic;                     -- E1 Channel 32 Data
    E1_CH33_RX_VAL  : out std_logic;                     -- E1 Channel 33 Data Valid
    E1_CH33_RX_DATA : out std_logic;                     -- E1 Channel 33 Data
    E1_CH34_RX_VAL  : out std_logic;                     -- E1 Channel 34 Data Valid
    E1_CH34_RX_DATA : out std_logic;                     -- E1 Channel 34 Data
    E1_CH41_RX_VAL  : out std_logic;                     -- E1 Channel 41 Data Valid
    E1_CH41_RX_DATA : out std_logic;                     -- E1 Channel 41 Data
    E1_CH42_RX_VAL  : out std_logic;                     -- E1 Channel 42 Data Valid
    E1_CH42_RX_DATA : out std_logic;                     -- E1 Channel 42 Data
    E1_CH43_RX_VAL  : out std_logic;                     -- E1 Channel 43 Data Valid
    E1_CH43_RX_DATA : out std_logic;                     -- E1 Channel 43 Data
    E1_CH44_RX_VAL  : out std_logic;                     -- E1 Channel 44 Data Valid
    E1_CH44_RX_DATA : out std_logic                      -- E1 Channel 44 Data
  );
end DEMULTIPLEXER_E3_TO_E1;
```

Demultiplexer : Interface Description

RESET

Asynchronous reset for the whole internal logic (E3 and the four E2 domains) of the demultiplexer.

E3_RX_CLK

Receive clock from the E3 line interface unit for the E3 demultiplexer. The whole logic of the demultiplexer works with this clock.

E3_RX_DATA

Serial RX data stream from the E3 line interface unit for the E3 demultiplexer.

E3_RX_LCV

Line Code Violation information from the E3 line interface unit (received data bit is invalid because of violation of the coding rules).

E3_RX_LOS

Loss Of Signal information from the E3 line interface unit (No receive signal available).

E3_RX_LOL

Loss Of Lock information from the E3 line interface unit (Receive signal frequency beyond the CDR frequency range).

E3_REF_CLK

Output of the E3 reference clock (Derieved from E3_RX_CLK).

E3_FRAME_START (E3_REF_CLK Synchronous)

This signaling output notifies the reception (first bit) of a frame. It reports this event by a 1 signal for a clock period.

E3_SYNC (E3_REF_CLK Synchronous)

Synchronization state output of the E3 deframer.
This output changes to 1 if three consecutive frames with error free frame alignment signals are received. It changes to 0 if four consecutive frames with errored frame alignment signals are received.

E3_RAI (E3_REF_CLK Synchronous)

Remote Alarm Indication output of the E3 deframer.
This output changes to 1 if the received RAI bits in the last four frames are at 1. It changes to 0 if the received RAI bits in the last four frames are at 0. The output is immediately updated, when the RAI bit is received. If the frame synchronization is lost, this output is reset to 0.

E3_NA (E3_REF_CLK Synchronous)

National Bit output of the E3 deframer.
The level at this output reflects the level of the received NA bit. The output is immediately updated, when the NA bit is received. If the frame synchronization is lost, this output is reset to 0.

E3_AIS (E3_REF_CLK Synchronous)

State output signal of the E3 deframer : Receiving Alarm Indication Signal (Idle '1').
The AIS output changes to 1 if four or less 0 bits are detected during the last two frame periods (2x 1536 bits). The AIS output changes to 0 if five or more 0 bits are detected during the last two frame periods (2x 1536 bits) or when frame synchronization could be achieved.

E3_LOS (E3_REF_CLK Synchronous)

State output signal of the E3 deframer : Receiving Loss Of Signal (Idle '0').
The LOS output changes to 1 if the inputs E3_RX_LOS or E3_RX_LOL changes to 1 or if 128 consecutive 0 bits are received. The LOS output changes to 0 if the inputs E3_RX_LOS and E3_RX_LOL are at 0 and if at least one 1 bit was received in the last 128 received bits.

E3_REMOTE_EN (E3_REF_CLK Synchron)

Activation input for the data transfer channel from the remote device. Set to 0 if not used.

E3_REMOTE_DATA (E3_REF_CLK Synchron)

Data transfer channel from the remote device. These four bits wide channel is transmitted in the E3 frame overhead instead of the first four justification control bits (C_{J1}). A nibble with new data is provided with every new frame, which can be noticed by the E3_FRAME_START signal.

E2_CH1_SYNC / E2_CH2_SYNC / E2_CH3_SYNC / E2_CH4_SYNC (E3_REF_CLK Synchronous)

Synchronization state outputs of the four E2 deframer.
This output changes to 1 if three consecutive frames with error free frame alignment signals are received. It changes to 0 if four consecutive frames with errored frame alignment signals are received.

E2_CH1_RAI / E2_CH2_RAI / E2_CH3_RAI / E2_CH4_RAI (E3_REF_CLK Synchronous)

Remote Alarm Indication outputs of the four E2 deframer.
This output changes to 1 if the received RAI bits in the last four frames are at 1. It changes to 0 if the received RAI bits in the last four frames are at 0. The output is immediately updated, when the RAI bit is received. If the E2 frame synchronization is lost, this output is reset to 0.

E2_CH1_NA / E2_CH2_NA / E2_CH3_NA / E2_CH4_NA (E3_REF_CLK Synchronous)

National Bit outputs of the four E2 deframer.
The level at this output reflects the level of the received NA bit. The output is immediately updated, when the NA bit is received. If the E2 frame synchronization is lost, this output is reset to 0.

E2_CH1_AIS / E2_CH2_AIS / E2_CH3_AIS / E2_CH4_AIS (E3_REF_CLK Synchronous)

State output signals of the four E2 deframer : Receiving Alarm Indication Signal (Idle '1').
The AIS output changes to 1 if four or less 0 bits are detected during the last two frame periods (2x 848 bits). The AIS output changes to 0 if five or more 0 bits are detected during the last two frame periods (2x 848 bits) or when frame synchronization could be achieved.

E2_CH1_LOS / E2_CH2_LOS / E2_CH3_LOS / E2_CH4_LOS (E3_REF_CLK Synchronous)

State output signals of the four E2 deframer : Receiving Loss Of Signal (Idle '0').
The LOS output changes to 1 if 128 consecutive 0 bits are received. The LOS output changes to 0 if at least one 1 bit was received in the last 128 received bits.

E1_CH11_RX_VAL / E1_CH12_RX_VAL / E1_CH13_RX_VAL / E1_CH14_RX_VAL /
E1_CH21_RX_VAL / E1_CH22_RX_VAL / E1_CH23_RX_VAL / E1_CH24_RX_VAL /
E1_CH31_RX_VAL / E1_CH32_RX_VAL / E1_CH33_RX_VAL / E1_CH34_RX_VAL /
E1_CH41_RX_VAL / E1_CH42_RX_VAL / E1_CH43_RX_VAL / E1_CH44_RX_VAL

Receive data valid signals (clock enable output) for the sixteen E1 RX interface channels.
Synchronized at the clock E3_REF_CLK. When this output is at 1 during the rising edge on the E3_REF_CLK output, the data bit at the corresponding channel data output is valid.
The nominal data rate for E1 is 2048 kbit/sec.
The outputs E1_CH1x_TX_VAL are connected to the first E2 demultiplexer.
The outputs E1_CH2x_TX_VAL are connected to the second E2 demultiplexer.
The outputs E1_CH3x_TX_VAL are connected to the third E2 demultiplexer.
The outputs E1_CH4x_TX_VAL are connected to the fourth E2 demultiplexer.

E1_CH11_RX_DATA / E1_CH12_RX_DATA / E1_CH13_RX_DATA / E1_CH14_RX_DATA /
E1_CH21_RX_DATA / E1_CH22_RX_DATA / E1_CH23_RX_DATA / E1_CH24_RX_DATA /
E1_CH31_RX_DATA / E1_CH32_RX_DATA / E1_CH33_RX_DATA / E1_CH34_RX_DATA /
E1_CH41_RX_DATA / E1_CH42_RX_DATA / E1_CH43_RX_DATA / E1_CH44_RX_DATA

Receive data output signals for the sixteen E1 RX interface channels.
Synchronized at the clock E3_REF_CLK. The data bit at this channel data output is valid, when the corresponding data valid signal is at 1 during the rising edge on the E3_REF_CLK output.
The nominal data rate for E1 is 2048 kbit/sec.
The outputs E1_CH1x_TX_DATA are connected to the first E2 demultiplexer.
The outputs E1_CH2x_TX_ DATA are connected to the second E2 demultiplexer.
The outputs E1_CH3x_TX_ DATA are connected to the third E2 demultiplexer.
The outputs E1_CH4x_TX_ DATA are connected to the fourth E2 demultiplexer.

Multiplexer / Demultiplexer : Used Ressources

Device	Multiplexer			Demultiplexer		
	Flip-Flops	4 bit – LUTs	Frequency	Flip-Flops	4 bit – LUTs	Frequency
XC2V250-4	1300-1400	1300-1400	> 150 MHz	600-650	900-950	> 150 MHz
XC3S200-4	1300-1400	1300-1400	> 140 MHz	600-650	900-950	> 150 MHz

The multiplexer requires such much logic because of the fully clock independent interfaces.

A multiplexer/demultiplexer unit requires about 60 % of a Xilinx® Spartan®-3 200 FPGA, which costs round about US$ 20.