

Metastability Characterization Report

Introduction

The setup and hold times of a register may deviate from ideal register behavior in actual applications as a result of finite circuit delays. A synchronization failure may occur if the data and clock do not satisfy the setup- and hold-time constraints of a flip-flop because the data is asynchronous with the clock. When asynchronous data changes inside the setup- and hold-time window, the resolution of the logic state by the flip-flop becomes less predictable. One measurable symptom of the problem is increased clock-to-out time. The increase in clock-to-out time depends on the time relationship between data and clock transitions. The susceptibility of a circuit to reach this metastable state can be described using a probabilistic equation. A description of this metastability equation follows in the next section.

Theory of Metastability

The following equation for metastability is written in terms of the mean time between failures and the clock-to-out settling time:

$$MTBF = (e^{(T_s/\tau)}) / (T_0 * f_d * f_c)$$

$$T_s = T_{co} + T_{met}$$

T_{co} = clock-to-out time

T_{met} = additional settling time, after the normal clock-to-out time, before sampling the output of the flip-flop.

τ = metastable decay constant

T_0 = metastability aperture at $T_{co} = 0$ ns

f_d = data transition rate (twice the data frequency, since there is a rising and falling edge in one period)

f_c = clock frequency

The aperture is defined as the window within a clock period that will cause the output settling time to be greater than a specified time, $T_{co} + T_{met}$, if the data signal changes. The aperture is calculated by recording the number of instances in which the clock-to-out time exceeds $T_{co} + T_{met}$ over a fixed number of cycles (the "operation time"). Bench tests (230 cycles) were performed to determine aperture for various Actel FPGAs. Note that the aperture decreases exponentially as the allowed settling time increases, which is an observable characteristic of flip-flops.

$$\text{Aperture} = T_0 * (e^{-(T_{co} + T_{met})/\tau})$$

Asynchronous data is assumed to have the same transition probability at any instant during a clock period. It follows that the probability of a single data transition occurring in the metastable aperture is the ratio of the aperture size to the clock period, or

$$p(\text{metastable transition}) = \text{aperture} / T_c$$

Mean Time Between Failures (MTBF) is defined as the operation time (230 cycles in these tests) divided by the number of errors. We compute the number of metastability errors in the following way: first, the probability of a metastable event occurring in a clock cycle is the number of data transitions per cycle multiplied by the probability of a data transition occurring during the metastable window, or

$$p = n * (\text{aperture} / T_c), \text{ where } n = \text{data transitions} / \text{cycle}$$

$$\text{or, } p = (f_d/f_c) * (\text{aperture} * f_c)$$

The number of clock cycles (N) in the operation time is the total time divided by the clock period, or

$$T_{\text{total}} / T_c = N$$

We can now write an equation for MTBF as follows:

$$MTBF = 1 / (\text{aperture} * f_d * f_c) = 1 / (T_0 * e^{-T_{co}/\tau} * f_d * f_c)$$

FPGA Metastability Characterization

We adjust the metastability equation to absorb the fixed $e^{T_{co}}$ term as FPGA manufacturers cannot directly measure the clock-to-out delay of a flip-flop.

$$MTBF = e^{C_2 * T_{met}} / C_1 * f_d * f_c$$

where T_{met} , f_d , and f_c are as defined earlier and

C_2 = metastability decay constant = $1 / \tau$.

C_1 = proportionality constant that is similar to T_0 (aperture)

There are several environmental and test condition factors that influence metastability characterization. These include the rise time of data and clock signals, input drive levels, operating voltage, temperature, stability, etc. Additionally, increased system noise due to switching of both internal nodes and I/Os can influence the metastability results. Therefore, it is essential to provide a quiet environment for testing.

Design Description

Figure 1 shows a schematic of the test circuit used to measure metastability in Actel devices. The normal propagation delay, operating under specified setup and hold time, is measured from the output of flip-flop 1 (DFF#1) to the input of flip-flop 3 (DFF#3) (see Figure 1). This value is

denoted by $T_{min} = T_{co} (DFF\#1) + t_{delay} + T_{su} (DFF\#3)$. This is the reference time to which the additional settling time, T_{met} , is added for characterization of metastability. T_{min} was obtained by comparing the outputs of flip-flops 1 and 3. The point at which their outputs no longer match is recorded as T_{min} .

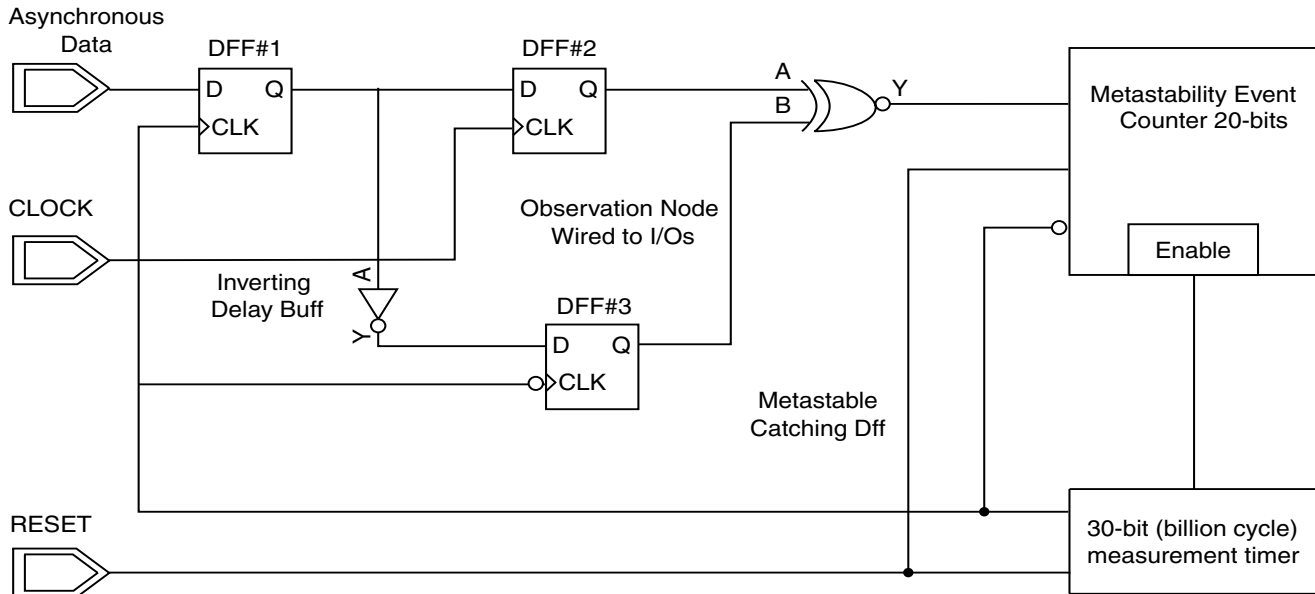


Figure 1 • Test Circuit

Flip-flop 2 (DFF#2) is clocked on the same edge as flip-flop 1. Conversely, flip-flop 3 must resolve the signal driven from the metastable flip-flop 1 before the falling clock edge. The inverting delay buffer was added to the path to avoid requiring an extremely narrow pulse width from the pulse generator. The propagation delay from the rising edge to the falling edge is defined as the design's T_{min} . The operating frequency must be limited so that all metastable events are resolved prior to the next rising edge. A detectable metastable event occurs when flip-flops 2 and 3 are in the SAME state. Under normal operating conditions flip-flops 2 and 3 are in opposite states due to the inverter in flip-flop 3's input path. The XNOR gate allows the event counter to record these metastable events.

After a billion clock cycles the counter is read, and the MTBF number is calculated.

This design was selected because $T_{min} + T_{met}$ was easily and accurately measured using an oscilloscope and pulse generator. $T_{min} + T_{met}$ is the difference between the rising edge and falling edges of the clock pulse generator. At a constant frequency one adjusts the duty cycle of the clock signal to find T_{min} . This procedure eliminates the need for absolute timing measurements, which require the selection of trip points – an additional source of error. Also, signal loading from scope probes can cause errors by reducing the

rise time. T_{met} is the additional time, expressed as a percentage of duty cycle change, relative to the normal propagation delay. Once T_{min} is found, additional T_{met} delay can be added for characterization purposes. T_{min} was resolved to within $\pm 0.01\%$ duty cycle at 10 MHz. This translates to an error of ± 10 ps.

The experimental setup is as follows:

- Clock and data inputs are driven from independent pulse generators (< 1 nS Rise time)
- Clock input levels are from 0V to 2.5V. These levels were required due to impedance matching requirements of our test fixture. Data input is driven 0V to 3.3V.
- Power supply settings were as follows:
 - SX, RTSX32 - $V_{CCA}, V_{CCI} = 3.3V, V_{CCR} = 5.0V$
 - ACT1 - $V_{CC}, V_{SV}, V_{PP} = 5.0, V_{KS} = 0V$
 - ACT2 - $V_{CC}, V_{SV}, V_{PP} = 5.0, V_{KS} = 0V$
 - ACT3 - $V_{CC}, V_{SV}, V_{PP} = 5.0, V_{KS} = 0V$
 - MX - $V_{CC}, V_{SV}, V_{PP} = 5.0, V_{KS} = 0V$

Metastability Parameters

Key equations

- $MTBF = (e^{(C_2 * T_{met})}) / C_1 * f_i * f_c$
- $\ln(MTBF) = C_2 * T_{met} - \ln(C_1 * f_i * f_c)$
- $y = m * X + b$

The plot of $\ln(MTBF)$ vs. T_{met} shows a linear relationship. C2 is the slope of the curve.

$$C_2 = (\ln(MTBF_1 / MTBF_2)) / (T_{met1} - T_{met2})$$

for any two data points. The y-intercept of the curve is given by $\ln(MTBF)$, and C1 is calculated with

$$C_1 = (e^{-b}) / (f_i * f_c)$$

Metastability Measurement Results

Our characterization data was taken from SX (0.35µm), RTSX32 (0.60µm), MX16 (0.45µm), ACT1 (1.0µm) and XL (0.6µm) devices. Theory says that C1 and C2 are independent of both the test frequency used and the data-to-clock-frequency ratio. The results concur within experimental tolerances. The plots of MTBF for the SX,

RTSX, MX, ACT1, and XL products include a plot for the ACT3 product as a reference. SX (0.35µm) demonstrates good improvement over ACT3. On the other hand, RTSX32 and MX16 are similar to ACT3 in metastability performance. Calculated coefficients are given in Table 1, while results are graphed in Figure 2. Figure 2 shows a metastability plot ($\ln(MTBF)$ vs. T_{met}) for several Actel families, using the experimental setup and equations previously described.

Table 1 • Metastability Coefficients for Actel FPGA Families

$f_c = 10\text{MHz}$		
Device Family	C1 (s)	C2 (1/s)
SX32 (0.35µm)	2.021E-11	1.2157E+10
RTSX32 (0.6µm)	3.933E-11	4.7342E+09
1460A(ACT3) (0.8µm)	5.570E-11	3.2700E+09
MX16 (0.45µm)	3.464E-10	3.4704E+09
1240XL(ACT2) (0.6µm)	3.16E-08	3.83E+09
1020A(ACT1) (1.0µm)	8.93E-09	2.35E+09

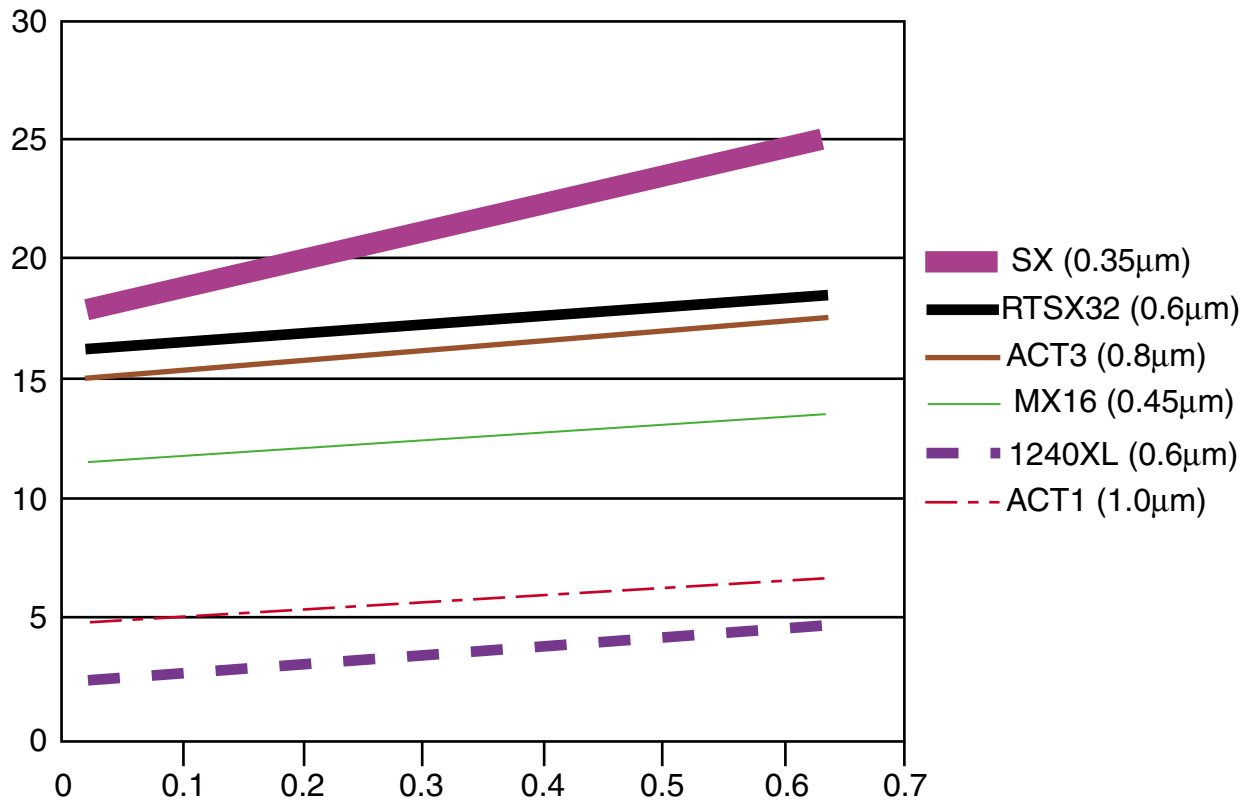


Figure 2 • Metastability Comparison of Actel FPGA Families

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