Fast On and Off Chip Delays with 1200XL and 3200DX I/O Latches

Introduction

Using Actel 1200XL and 3200DX devices, latched I/O buffer macros can improve clock input-to-registered-output performance. Latched I/O buffer macros also increase the speed of latching signals into the FPGA. Flip-flops created from these I/O latch macros improve performance by up to 22 percent compared with traditional approaches. The ACTgen Macro Builder tool from Actel automatically generates I/O registers using this technique. This application note c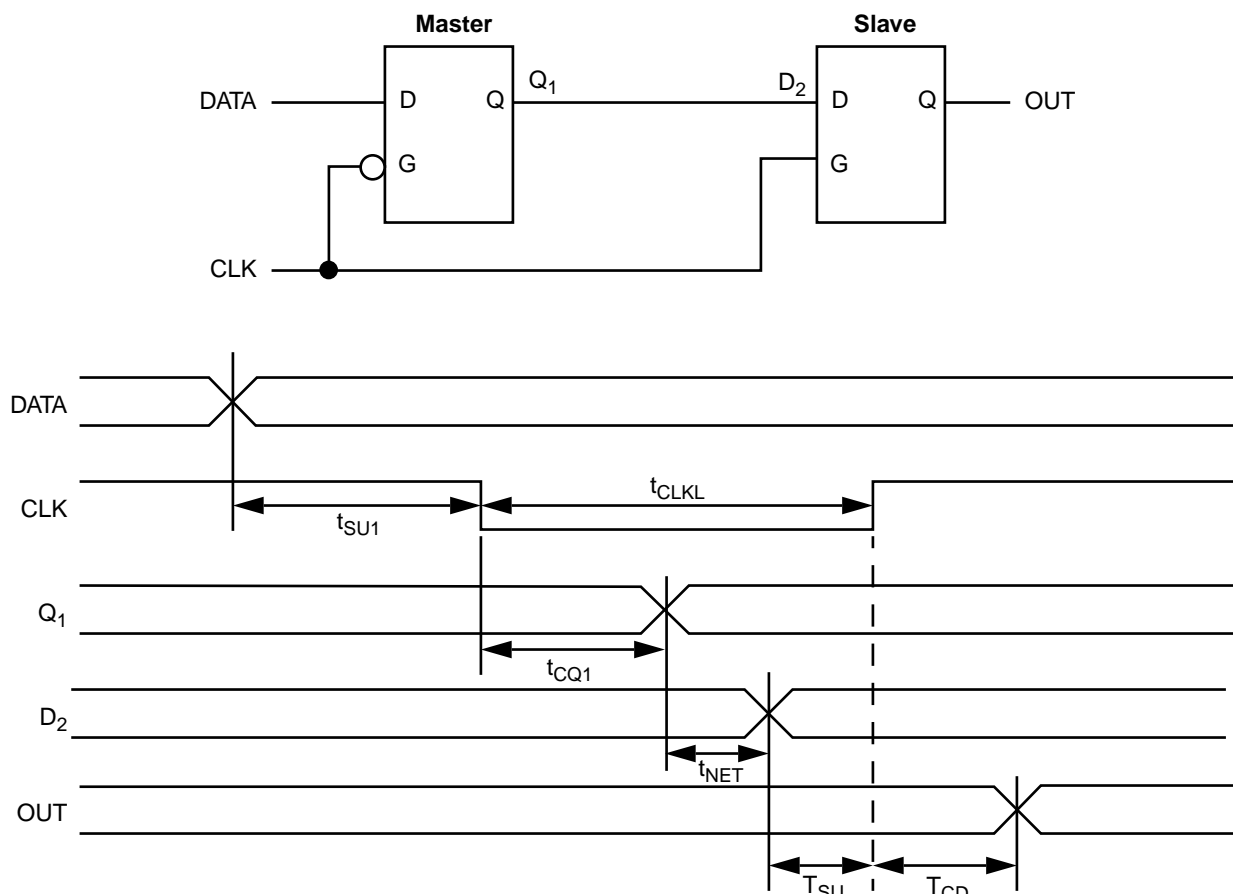ompares the use of traditional approaches with the use of I/O latch macros in 1200XL and 3200DX designs for the designer interested in the details.

Master/Slave Flip-Flops

As shown in Figure 1, two level-sensitive latches can be combined to create a positive edge-sensitive flip-flop.

Where:

1. $T_{CO} = t_{CO2}$

2. $T_{SU} = t_{CKL} - t_{CO1} - t_{RD1} > t_{SU2}$

3. t_{SU2} = minimum setup time for slave
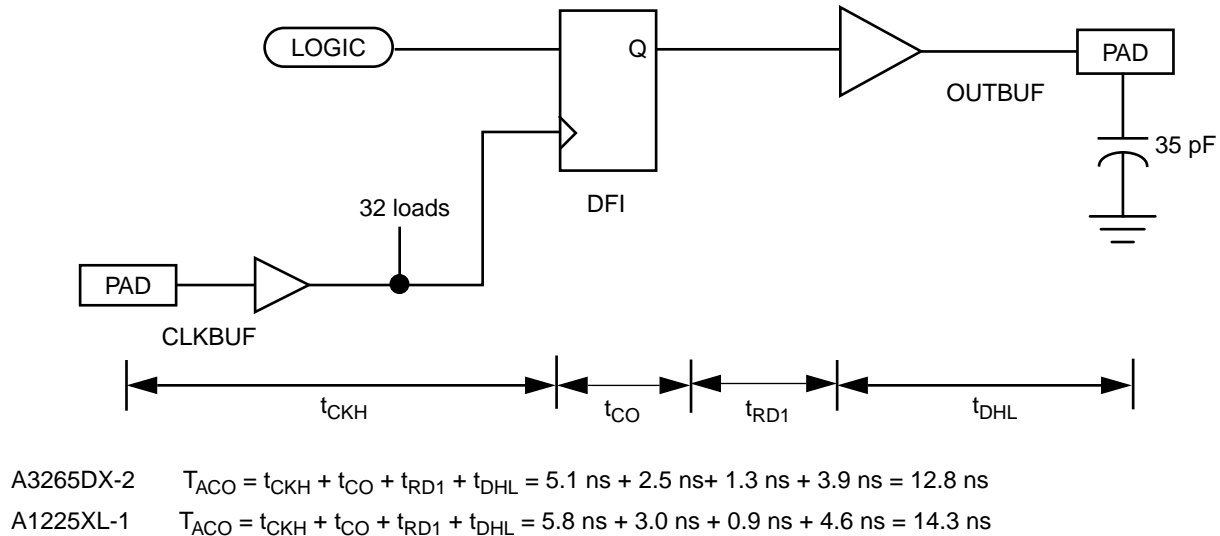

Figure 1 • *Master/Slave Flip-Flop*

The clock-to-output delay of the resulting flip-flop is determined by the clock-to-output delay of the slave latch. The clock period low time (t_{CKL}) must be greater than the clock-to-output delay of the master latch (t_{CO1}) plus the net delay from the master latch output (t_{RD1}) plus the setup time of the slave latch (t_{SU2}).

Constructing Registered Outputs

You can construct a registered output by combining a flip-flop macro with an output buffer as depicted in Figure 2. The clock-to-out delay for an A3265DX-2 under worst-case commercial conditions is 12.8 ns. For the A1225XL-1 under worst-case commercial conditions, clock-to-out delay is 14.3 ns.
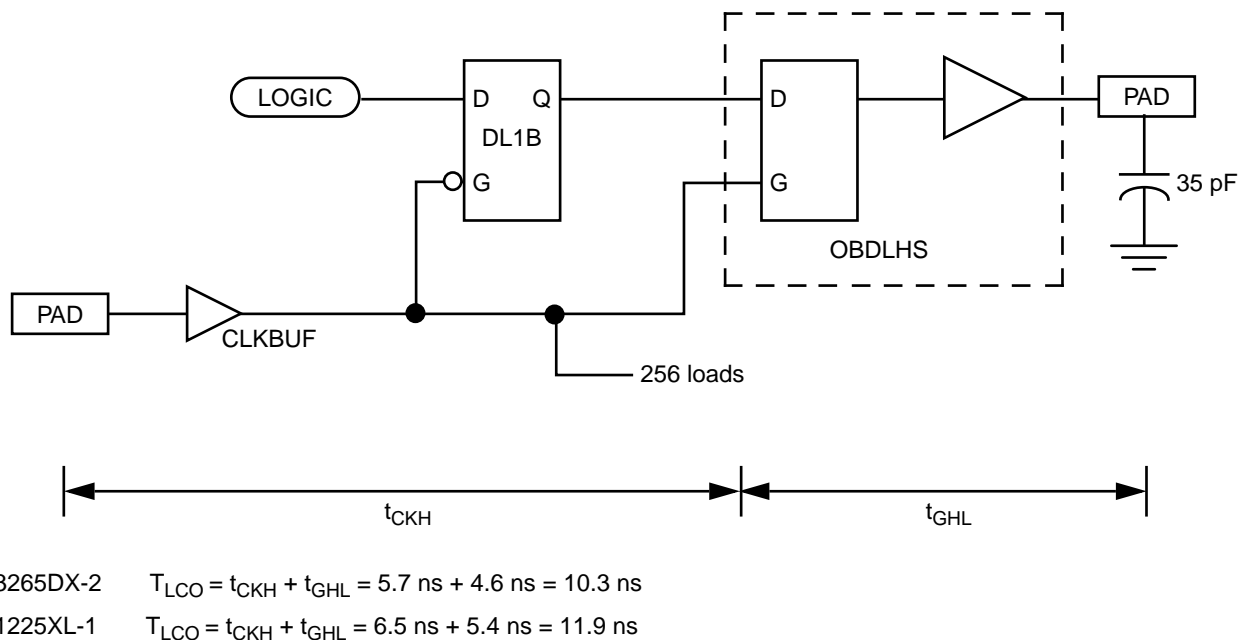

$$T_{ACO} = t_{CKH} + t_{CO} + t_{RD1} + t_{DHL}$$

A3265DX-2 $T_{ACO} = t_{CKH} + t_{CO} + t_{RD1} + t_{DHL} = 5.1 \text{ ns} + 2.5 \text{ ns} + 1.3 \text{ ns} + 3.9 \text{ ns} = 12.8 \text{ ns}$

A1225XL-1 $T_{ACO} = t_{CKH} + t_{CO} + t_{RD1} + t_{DHL} = 5.8 \text{ ns} + 3.0 \text{ ns} + 0.9 \text{ ns} + 4.6 \text{ ns} = 14.3 \text{ ns}$

Figure 2 • *Conventional Registered Output*

I/O Latch Flip-Flops

You can also construct a registered output as a master/slave flip-flop using a logic module latch (DL1B) and a latched output buffer (OBDLHS) as shown in Figure 3.

In this case, the clock-to-out delay for an A3265DX-2 device under commercial worst-case conditions is 10.3 ns. In this case, the loading on the global clock network is assumed to be 256 loads. For similar conditions, the A1225XL-1 has a clock-to-out delay of only 11.9 ns.

A3265DX-2 $T_{LCO} = t_{CKH} + t_{GHL} = 5.7 \text{ ns} + 4.6 \text{ ns} = 10.3 \text{ ns}$

A1225XL-1 $T_{LCO} = t_{CKH} + t_{GHL} = 6.5 \text{ ns} + 5.4 \text{ ns} = 11.9 \text{ ns}$

Figure 3 • *Master/Slave Registered Output*

Registered inputs can also be constructed using a logic module latch (DL1) with a latched input buffer macro (IBDL) as shown in Figure 4. This is equivalent to the I/O macro, IR. Data can be latched into the FPGA most efficiently in this configuration. Because of the unique architecture of the I/O buffer latches in 1200XL and 3200DX families, the input latch has zero external setup time. This means that the data may change just before the rising edge of the clock signal. Data must be held at the input of the latch for the time t_{HEXT}.
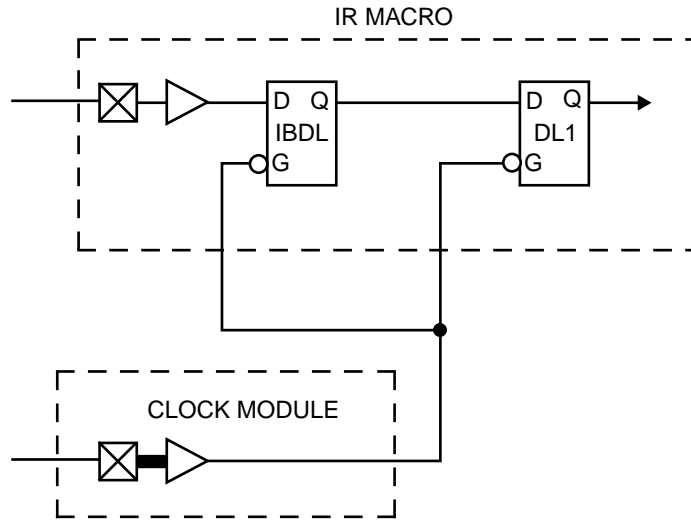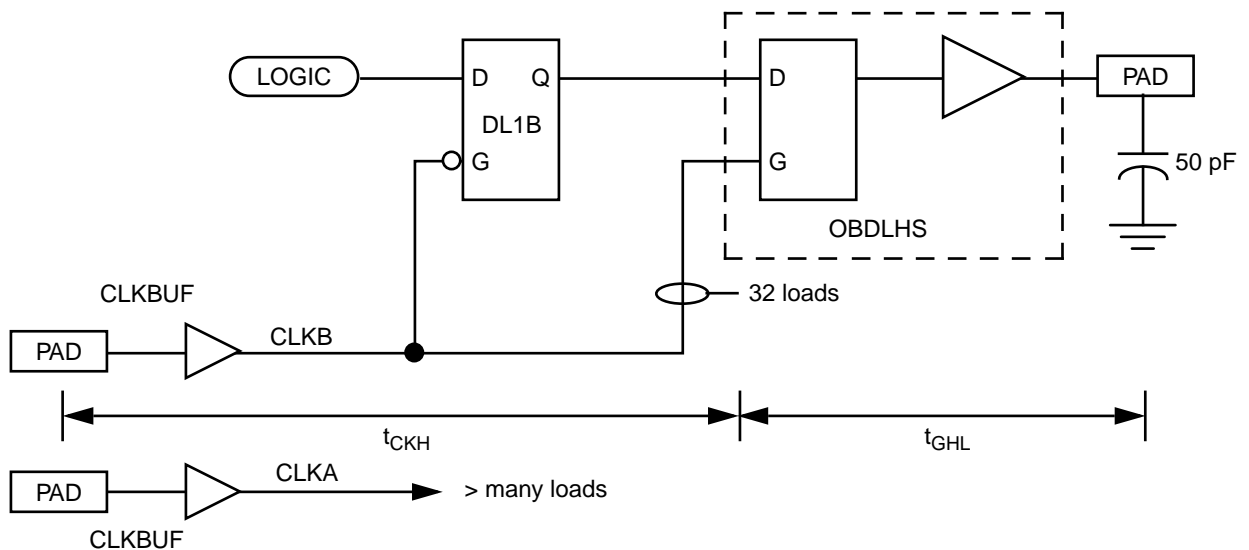

Figure 4 • *Master/Slave Registered Input*

Dual Clock Approach

Faster clock-to-out can be achieved by utilizing the second global clock network as an I/O clock. In this configuration, shown in Figure 5, CLKA drives the synchronous circuitry on the device and CLKB drives the I/O master/slave latches. Both clock networks are operating at the same frequency and must be connected together outside of the devices. In this case, a 9.7 ns clock-to-out delay can be achieved for the A3265DX-2 and 11.2 ns for the A1225XL-1.

Alternately, an INBUF can be used to drive the I/O latch, if fanout on the INBUF is kept less than four to achieve similar performance.

A3265DX-2 $T_{CO} = t_{CKH} + t_{GHL} = 5.1 \text{ ns} + 4.6 \text{ ns} = 9.7 \text{ ns}$

A1225XL-1 $T_{CO} = t_{CKH} + t_{GHL} = 5.8 \text{ ns} + 5.4 \text{ ns} = 11.2 \text{ ns}$

Figure 5 • *Dual Clock Master/Slave Registered Output*

Implementation Rules

Actel strongly suggests following these rules when constructing flip-flops with the I/O latches:

1. Use ACTgen Macro Builder to automatically create I/O registers implemented with I/O latches. You need not design them yourself. This can save a lot of time and allows you to focus on more important issues with your design.

2. Do not put combinatorial macros in the data path between master and slave latches. Added delay may prevent the flip-flop from operating properly. For inputs, combinatorial macros are allowed in the data path between the master and slave latches *only* if the logic module latch and the combinatorial latch are both combinable hard macros.

3. For outputs, do not connect the master latch output to any loads except the I/O latch D input.

4. Use a latch made from sequential logic modules for the master stage for outputs on the slave stage for inputs. Sequential module latches have better timing characteristics. They also allow combining to take place, which can improve the performance of the data being registered. The transparent-low sequential module latches are DL1B and DL1C.

5. Use net criticality to ensure that the net delay does not violate the setup requirements of the slave latch (as defined in Figure 1). Verify the timing conditions after place and route is complete. Note that an asymmetrical duty cycle on the clock signal (less than 50% low time) will provide more tolerance on the allowable net delay between latches.

6. Design to combine. The Designer Series System will automatically combine combinatorial logic into the D input of the DL1B latch if the combiner rules are met.